

**IMAGE SYSTEM CONTROLLER**  
**USER'S MANUAL**

KEITHLEY/METRABYTE CORP.

DOC. 79040

# CONTENTS

<i>Section</i>		<i>Page</i>
<b>1</b>	<b>Introduction</b>	<b>1-1</b>
1.1	Features	1-1
<b>2</b>	<b>Pinout and Signal Description</b>	<b>2-1</b>
<b>3</b>	<b>Architecture</b>	<b>3-1</b>
3.1	Host Interface	3-1
3.2	Arbiter	3-1
3.3	Address Generator	3-2
3.4	VRAM Controller	3-2
3.5	Display Timing Generator	3-4
3.6	Display Update Generator	3-5
<b>4</b>	<b>Programmable Registers</b>	<b>4-1</b>
4.1	Register Values After Reset	4-2
4.2	Host Interface Registers	4-2
4.3	Display/Acquire Control Registers	4-8
4.4	Video Timing Registers	4-9
4.5	Address Generator Registers	4-11
<b>5</b>	<b>Host and Memory Interface Operations</b>	<b>5-1</b>
5.1	Arbitration	5-1
5.2	Internal Register Access	5-1
5.3	Display Update Cycle	5-3
5.4	CAS-before-RAS Refresh Cycle	5-4
5.5	Host Direct Cycle	5-5
5.6	X-Y Indirect Cycle	5-6
5.7	Read/Write Transfer Cycle	5-6
5.8	Fast Page Mode	5-7
5.9	RDY interface	5-8
5.10	Reset and Initial Setup	5-9
<b>6</b>	<b>Display and Acquire Control</b>	<b>6-1</b>
6.1	Auto-Acquire	6-1
6.2	Internally Generated Video Signals	6-1
6.3	External Sync Modes	6-3
<b>7</b>	<b>Specifications</b>	<b>7-1</b>
<b>8</b>	<b>Real-Time Processing with the ISC</b>	<b>8-1</b>

# 1. INTRODUCTION

The Image System Controller (ISC) is designed in 1.5 micron CMOS. The primary function of the ISC is that of a VRAM controller. Unlike generic VRAM controllers for graphics applications, the ISC is optimized for both acquisition and display control. The ISC is designed to work with both 256K and 1 MEG VRAMs. In addition to providing all the necessary video timing and display update control, the ISC also provides flexible address generation to fit a variety of VRAM architectures. The ISC has a 16 MEG direct address space as well as a block address mode for a smaller 64K address space. Although designed as a VRAM controller, the ISC can be used as a DRAM controller as well. Two very important features of the chip are auto-acquisition which allows single or multiple acquires by simply toggling a pin and real-time processing mode which creates and coordinates all the timing signals necessary to perform frame rate pixel processing.

## 1.1 FEATURES

The ISC is highly programmable and supports a broad range of display resolutions and memory architectures. The following are the major ISC features:

- Generates all of the necessary VRAM/DRAM control signals for 256 K and 1 MEG devices.
- Synchronizes to external video sources as well as internally generates all video signals necessary for display including composite sync and blank.
- Supports interlaced and non-interlaced video with vertical wrap around for line scan applications.
- Automatically generates address and control signals for display/acquire update cycles.
- Addressing space of 16 MEG in either one-for-one direct, 64 K at a time block mode or X-Y addressing with a four bit code for registered mapped applications.
- Provides multiple step sizes for X-Y addressing for greater flexibility of memory architectures and the ability to move around an image by steps of more than one pixel at a time.
- Allows fast page mode cycles.
- CAS-before-RAS burst DRAM refresh.
- Automatically acquires one or many frames with a simple pulse(s) to a pin.
- Automatically generates all address and control signals for real-time processing at frame rates.
- Provides arbitration between internally generated memory cycles and host initiated cycles.
- Automatically reformats data when image is acquired via the serial access port of a bank-by-four memory architecture.
- Enables host controlled read and write transfers between DRAM and SAM.
- Automatically reformats data for images acquired via the serial access port with a bank-by-four memory architecture.

## 2. PINOUT and SIGNAL DESCRIPTION

Figure 2.1 shows the signal names and pin numbers for the 84 pin package of the ISC. A description of the signals is given in Table 2.1.

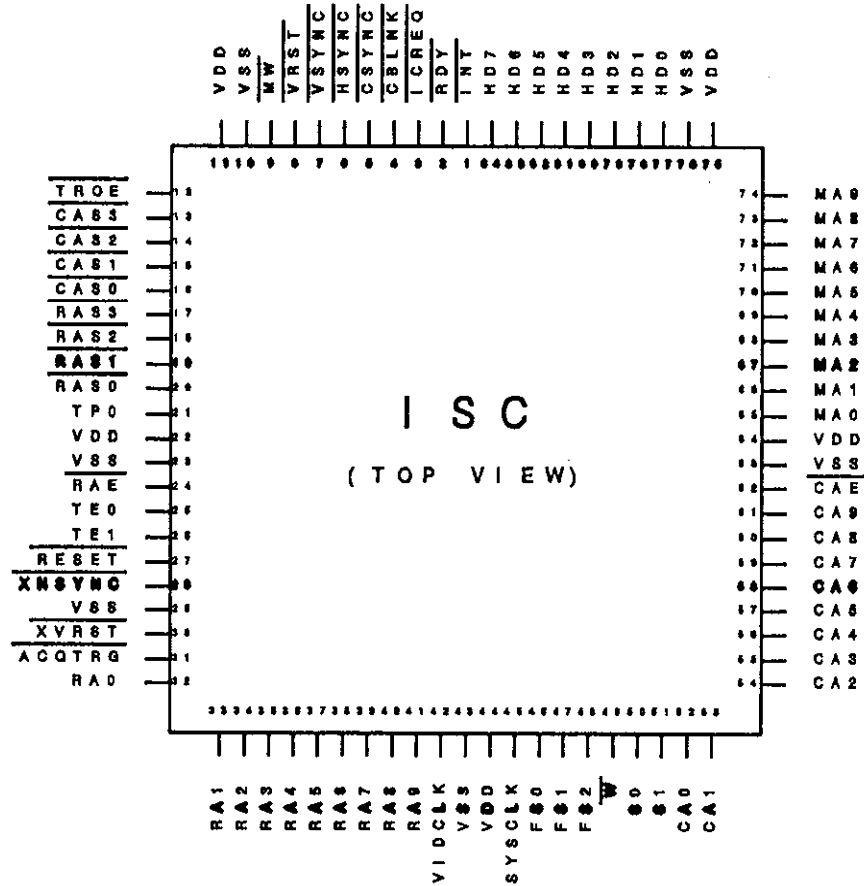


Figure 2.1. Pin Assignment and Signal Names

The ISC is packaged in an 84 pin J-lead plastic chip carrier (PLCC).

SIGNAL	PIN	I/O	DESCRIPTION
MA9-MA0	74-65	O	Memory Address 9-0 These ten memory address outputs multiplex between ROW address at RAS time and COL address at CAS time. They are further multiplexed internally for display update address, X-Y address, host direct address or all 0's CAS-before-RAS refresh. These outputs are designed to drive VRAM/DRAM directly but a buffer is recommended for driving large or many banks of memory.
RA9-RA0	41-32	I	Row Address 9-0 These ten address pins are multiplexed to the memory address pins at RAS time during a host direct, read transfer or write transfer memory access. The Row address is latched on ~RAE going low.
CA9-CA0	61-52	I	Col Address 9-0 These ten address pins are multiplexed to the memory address pins at CAS time during a host direct, read transfer or write transfer memory access. The Col address is latched on ~CAE going low. During an X-Y address cycle, the four LSB's of these pins determine the X-Y function adjust.
S1,S0	51,50	I	Select RAS/CAS 1,0 These two select pins are user programmable to select either or both of Row address selects (RAS) and Col address selects (CAS) during a host direct, read transfer or write transfer memory access. Select is latched on ~CAE going low.
~RAE	24	I	Active Low Row Address Enable The high-to-low transition of RAE latches RA9-RA0 and FS2-FS0 and initiates a host access cycle. During an X-Y address cycle the Row address register is updated on the rising edge of RAE. RAE is synchronous with SYSCLK and must meet setup and hold requirements.
~CAE	62	I	Active Low Col Address Enable The high-to-low transition of CAE latches CA9-CA0 and S1,S0. During an X-Y address cycle the Col address register is updated on the rising edge of CAE. CAE is synchronous with SYSCLK and must meet setup and hold requirements.
~W	49	I	Read/Write During non-SAM transfer host initiated memory cycles, ~W determines the direction of data transfer and the state of the memory write pin (~MW). Also, during an internal register access, ~W determines if data is to be read from or written to an internal register.
~INT	1	O	Active Low Interrupt Request This output indicates that a previously enabled interrupt condition has occurred. This signal will remain active until the internal status register has been read. Four independent conditions may trigger an

interrupt, the end of an acquisition, a display update or refresh error or that a previously selected scan line has been reached.

SIGNAL	PIN	I/O	DESCRIPTION
~RDY	2	O	<p>Active Low Ready</p> <p>Under normal circumstances, this pin is at a high impedance state. At the beginning of a host access (~RAE&gt;LOW), the ready pin goes high and remains high until the ISC recognizes the host initiated cycle AND the user defined wait state has been reached. At this point the ready pin will go low and remain low until ~RAE goes high.</p>
~ICREQ	3	O	<p>Active Low Internal Cycle Request</p> <p>This output indicates that an internal cycle is pending (display update or refresh). This pin will remain LOW until the internal cycle has been serviced.</p>
HD7-HD0	84-77	BI	<p>Host Data Bus 7-0</p> <p>The internal registers of the ISC are accessed via these eight bi-directional data pins. Setup and hold times relative to ~CAE must be observed.</p>
FS2-FS0	48-46	I	<p>Function Select 2-0</p> <p>These three bits form the function select code that determine the type of cycle requested by the host processor. These bits are latched on ~RAE going low and must meet the specified setup and hold times.</p>
SYSClk	45	I	<p>System Clock</p> <p>The system clock is used to generate all memory timing signals. All host interface signals must be synchronous to SYSClk.</p>
~RESET	27	I	<p>Active Low Reset</p> <p>The Reset puts all of the ISC's internal registers and counters and output signals to a known state. Reset must be held low for a minimum of three SYSClk periods. After Reset has been released, the ISC puts out a burst of eight CAS-before-RAS refresh cycles every 512 SYSClk periods until the internal registers are re-programmed.</p>
~ACQTRG	31	I	<p>Active Low Acquire Trigger</p> <p>This pin is used to enable displays and acquires. When this signal is pulsed low, the ISC waits for the beginning of the next frame, acquires/displays the frame and then sets the End Acquire bit in the status register. If ~ACQTRG is held low, the ISC will continuously display/acquire.</p>

SIGNAL	PIN	I/O	DESCRIPTION
~RAS3~RAS0	17-20	O	<p>Active Low Row Address Strobe 3-0</p> <p>These outputs drive the ~RAS inputs to VRAM/DRAM. The operation of these pins are controlled by the ISC control registers. If bit 13 of control register A is set, the source of control is the S1 and S0 input pins during a host direct, read transfer or write transfer memory cycle. If bit 15 of control register B is set, the source of control for these outputs is the block mode register for these cycles. If bit 11 of control register A is set, then all four RAS outputs will become active for all host initiated memory cycles. During an X-Y address cycle (if bit 11 of control register A is NOT set) the source of control for these outputs is the X-Y address register. During an internal display update cycle, the source of control is normally the display address register. If bit 11 of control register B is set, then all four RAS outputs become active during a display update cycle. During a CAS-before-RAS refresh cycle, all four RAS outputs become active.</p>
~CAS3~CAS0	13-16	O	<p>Active Low Col Address Strobe 3-0</p> <p>These outputs drive the ~CAS inputs to VRAM/DRAM. The operation of these pins are controlled by the ISC control registers. If bit 12 of control register A is set, the source of control is the S1 and S0 input pins during a host direct, read transfer or write transfer memory cycle. If bit 15 of control register B is set, the source of control for these outputs is the block mode register for these cycles. If bit 10 of control register A is set, then all four CAS outputs will become active for all host initiated memory cycles. During an X-Y address cycle (if bit 10 of control register A is NOT set) the source of control for these outputs is the X-Y address register. During an internal display update cycle, the source of control is normally the display address register. If bit 10 of control register B is set, then all four CAS outputs become active during a display update cycle. During a CAS-before-RAS refresh cycle, all four CAS outputs become active.</p>
~MW	9	O	<p>Memory Write</p> <p>This output drives the Write Enable inputs to VRAM/DRAM. During a non-SAM transfer host initiated memory cycles, this output follows the ~W input pin. During a SAM transfer cycle, the state of this output is determined by the Function Select Codes. During an internal display update memory cycle, the state of this pin is determined by bit 12 of control register B. During a CAS-before-RAS refresh cycle, this output remains high.</p>
~TROE	12	O	<p>Active Low Shift Register Transfer and Output Enable</p> <p>This output drives the ~TROE input of VRAM or the ~OE input of DRAM. During a non-SAM transfer host initiated memory cycle,</p>

the state of this output is determined by the  $\sim W$  input pin. During a SAM transfer memory cycle, the state of this pin is determined by the Function Select pins. During an internal display update memory cycle, the state of this pin is determined by bit 12 of control register B. During a CAS-before-RAS refresh cycle, this output remains high.

SIGNAL	PIN	I/O	DESCRIPTION
$\sim$ CBLNK	4	O	<p>Active Low Composite Blank</p> <p>This output controls the display blanking to a monitor. <math>\sim</math>CBLNK is driven low during both horizontal and vertical blanking times. The duration of both horizontal and vertical blank is programmable. Setting bit 0 of control register B to a zero will cause the entire screen to be blanked.</p>
$\sim$ CSYNC	5	O	<p>Active Low Composite Sync</p> <p>In interlaced mode ( control register B, bit 4 equals 1 ), this signal controls the vertical retrace of a monitor so that proper field alignment is obtained. Both American NTSC and European PAL standards are supported. The user can choose the standard by programming bit 3 of control register B to the appropriate value. When bit 4 of control register B is set to zero, the ISC is in NON-interlaced mode and the composite sync signal simply follows the HSYNC signal.</p>
$\sim$ HSYNC	6	O	<p>Active Low Horizontal Sync</p> <p>This signal is used to control the horizontal retrace of a monitor. The timing of this signal is user programmable.</p>
$\sim$ VSYNC	7	O	<p>Active Low Vertical Sync</p> <p>This signal is used to control the vertical retrace of a monitor with separate sync inputs. In interlaced mode, this signal will go low at the beginning of the Broad pulses of the composite sync signal. In NON-interlaced mode, this signal will go low at the same time that the internal vertical line counter is reset, at the end of a frame. In either case, the duration of this pulse is user programmable.</p>
$\sim$ VRST	8	O	<p>Active Low Vertical Reset</p> <p>This signal occurs once at the beginning of each frame. Its primary use is to frame sync one ISC to another.</p>
$\sim$ XHSYNC	28	I	<p>Active Low External Horizontal Sync</p> <p>This input is used to synchronize the horizontal timing of an ISC to an outside horizontal sync source. This input would normally be used with the external vertical reset input signal. Bit 2 of control register B determines whether the ISC generates HSYNC internally or uses this signal to slave to.</p>
$\sim$ XVRST	30	I	<p>Active Low External Vertical Reset</p> <p>This signal is used to synchronize the vertical timing of an ISC to an outside frame sync signal. This signal must occur only once at the</p>



beginning of each frame. This signal would normally be used alone to genlock to an outside video source or together with the ~XHSYNC in a master/slave ISC configuration. Bit 1 of control register B determines whether the ISC generates vertical signals internally or uses this input signal to slave to.

SIGNAL	PIN	I/O	DESCRIPTION
TE1,TE0	26,25	I	Internal Test Enable 1,0 These two test signals are used in the production of the ISC and are for internal use only. THESE TWO PINS MUST BE TIED TO GROUND FOR THE CHIP TO WORK.
TP0	21	O	Internal Test Point This test point is used in the production of the ISC and is for internal use only. THIS PIN MUST REMAIN UNCONNECTED.
VDD	11,22,44 64	+	+5 volt supply
VSS	10,23,29 43,63	-	Ground

# ARCHITECTURE

The Image System Controller consists of six functional blocks (Figure 3.1):

- Host Interface
  - Control and Status Registers
  - Address and Control Latches
- Arbiter
- Address Generator
  - Address Registers
- VRAM Controller
  - Refresh Controller
  - Address Multiplexer
- Display Timing Generator
  - Horizontal Timing Control
  - Composite Sync Timing Control
  - Vertical Timing Control
  - Vertical Interrupt Control
- Display Update Generator
  - Display Update Registers

## 3.1 HOST INTERFACE

The host interface contains the two control registers, the status register, the address latches and the internal register address decoders.

Control registers A and B are 16 bit host programmable registers that dictate the ISC's mode of operation. Each register may be read from or written to by the host. See section 4. for detailed information.

The status register consists of four bits and is read only. After this register has been read from the host, the contents are automatically cleared. The four conditions that may set a bit in this register are: The end of an acquisition, a display update error, a refresh error or a vertical interrupt. An interrupt may be sent to the host on the  $\sim$ INT pin by setting the appropriate interrupt enable bit in control register B.

There are two address latches. The first address latch latches RA9-RA0 and FS2-FS0 on the high-to-low transition of  $\sim$ RAE. The second address latch latches CA9-CA0 and S1,S0 on the high-to-low transition of  $\sim$ CAE.

## 3.2 ARBITER

The Arbiter determines whether a host initiated cycle, an internally generated display update cycle or an internally generated burst refresh cycle will be performed. Priority is granted as follows:

- Any cycle in progress
- A display update cycle (if enabled)
- A burst refresh cycle (if enabled)
- A host initiated cycle

When an internal cycle is in progress, a host initiated cycle is held-off with the  $\sim$ RDY pin remaining

high until the internal cycle(s) is complete. The host may observe the request for an internal cycle by monitoring the  $\sim$ ICREQ pin. This Internal Cycle Request pin will go low when the ISC would like to perform a display update or burst refresh and will remain low until the request has been serviced.

### 3.3 ADDRESS GENERATOR

The address generator consists of the X-Y ROW address register, The X-Y COL address register and the block address register. The address generator provides X-Y addressing for use in designs that may be register mapped, block mode direct addressing for use in designs that have an address space limited to 64K and fast page mode column addressing that is synchronized with the display update address generator for real-time processing or limited acquisition into DRAM. The address generator provides address linearization called Reformat. Address Reformat is necessary when interlaced data has been acquired into VRAM through SAM in a "bank-by-four" memory architecture. Reformat may be invoked by setting bit 14 of control register A.

X-Y addressing allows the user to move through DRAM using only a four bit code presented at CA3-CA0. The independent ROW and COL functions available are NOP, INCRement, DECReament and CLearR. The user may step through memory by increments of more than one by programming the X-Y ROW STEPSIZE and X-Y COL STEPSIZE bits of control register A (bits 5 - 0). The ROW and COL STEPSIZE adjustments are also useful in mapping video lines and pixels to memory rows and columns for many different memory architectures. Fast page mode may be used with X-Y addressing by the user toggling  $\sim$ CAE to create Column Address Strokes and holding  $\sim$ RAE low for the duration of the cycle. The user must insure however, that a row boundary not be exceeded for the duration of the  $\sim$ RAE cycle. NOTE that since the ROW portion of the X-Y address register is updated on the rising edge of  $\sim$ RAE and the COL portion is updated on the rising edge of  $\sim$ CAE, the two rising edges  $\sim$ RAE and  $\sim$ CAE must occur within the same SYSCLK cycle to insure that the ROW address adder recognizes a carry out from the COL address adder.

The Block Address Register (BAR) is a user programmable register that allows the user to directly address memory in 64K portions at a time. The BAR contains the two MSB's each of the row and column address registers and the two bits each that make up the row selects (RS1-RS0) and the column selects (CS1-CS0). NOTE that the contents of this register may be altered after an X-Y addressing operation. NOTE also that register values RA9 and CA9 are static and will not change with an X-Y address cycle.

When programmed for real-time mode, the address generator automatically creates the column portion of the DRAM address with the row portion of the address coming from the display update generator. The address generator is automatically CLEARED each time a display update is performed, thus resetting the pixel count to the beginning of a line. The column address is incremented each time  $\sim$ CAE is toggled high. A gated version of the pixel clock may be used for  $\sim$ CAE in this mode. The length of the cycle is determined by  $\sim$ RAE and a delayed version of  $\sim$ CBLNK may be used to create  $\sim$ RAE. The direction of data to DRAM is determined by the  $\sim$ W pin. In this mode, the system clock to the ISC must be replaced with the pixel clock.

### 3.4 VRAM CONTROLLER

The VRAM controller has no programmable registers but contains the address multiplexers, the burst refresh controller and the VRAM signal timing generator.

The address multiplexer provides the VRAM/DRAM array with row and column addresses at the proper time. Its input comes from the row, column and select pins, the X-Y address generator and the display update generator.

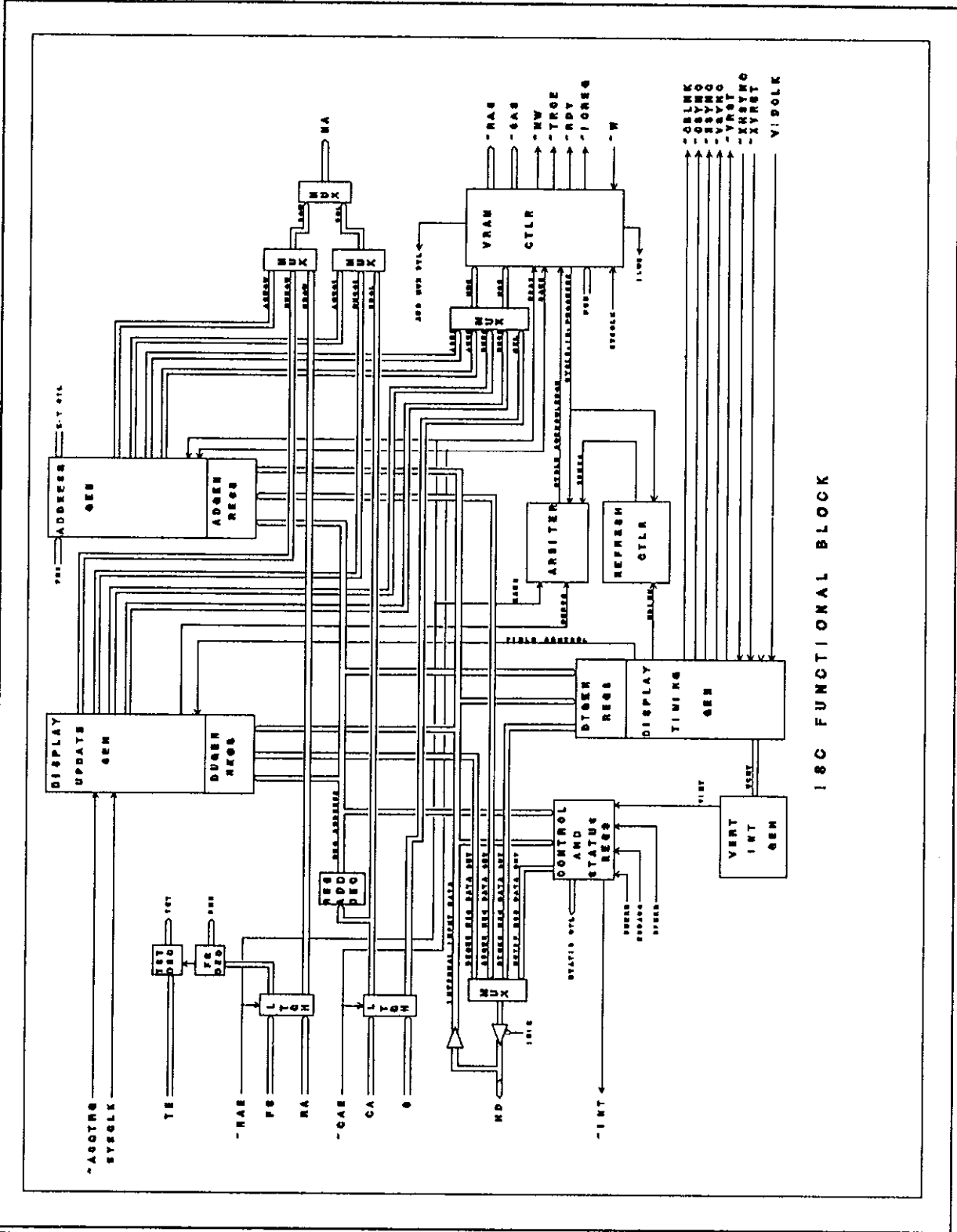


Figure 3.1 ISC Internal Architecture Block Diagram

The burst refresh controller initiates a burst of CAS-before-RAS refresh cycles at the beginning of composite blank by sending a refresh cycle request to the arbiter. After the arbiter acknowledges the refresh request, the burst refresh counter counts the number of refresh cycles until the programmed refresh burst length is reached (control register A, bits 8 and 9). When the beginning of the last refresh in a burst is reached, the refresh controller takes away the refresh request.

The VRAM signal timing generator creates the following VRAM/DRAM signals at the proper time:  $\sim$ RAS(3-0),  $\sim$ CAS(3-0),  $\sim$ TROE and  $\sim$ MW. The internal signals "Cycle-In-Progress" (CYIP) and "Busy" are also created by this circuit. The CYIP signal lets the arbiter know when a memory cycle is in progress. The Busy signal controls the external  $\sim$ RDY signal and its duration is dependent on the value of the wait state limit of control register A, bits 7 and 6.

### 3.5 DISPLAY TIMING GENERATOR

The Display Timing Generator consists of the Horizontal timing control, Composite Sync timing control, Vertical timing control and the Vertical interrupt control.

The Horizontal timing generator creates the Horizontal Sync signal and the Horizontal Blank portion of the Composite Blank signal. The Horizontal control consists of the following registers:

- Horizontal Total Latch
- Horizontal End Sync Latch
- Horizontal Start Blank Latch
- Horizontal End Blank Latch
- Horizontal Counter

The Horizontal latches are user programmable and may also be read by the host. The Horizontal counter is read only. Reading the Horizontal counter is of little use since its value changes often and is asynchronous to the system. Its read-back use is mainly for manufacturing test. The first two Horizontal latches determine the scan line length and horizontal sync duration respectively. The second two latches determine the beginning and end of horizontal blank respectively. The Horizontal counter increments its value on every rising edge of VIDCLK and resets the clock cycle after HTOTAL is reached. The Horizontal Timing Controller also provides mid-line information to the Vertical Timing Generator for interlaced display and synchronizes the Horizontal timing signals to an external Horizontal sync signal.

The Composite timing controller creates the Composite Sync signal. The Composite Sync controller consists of the composite sync counter, the pulse width extraction circuit and the beginning of vertical count decoder. The composite sync counter counts out the equalizing and broad pulse widths of composite sync. This counter is read only to the host and its read-back capabilities are mainly intended for manufacturing test. The pulse width extraction circuit contains an arithmetic unit that automatically calculates the equalizing and broad pulse widths from the values in the HTOTAL and HENDSYNC latches. The beginning of vertical count decoder determines when to begin and end the equalizing and broad pulses.

The Vertical timing generator creates the vertical reset signal, vertical Sync signal and the Vertical Blank portion of the Composite Blank signal. The Vertical control consists of the following registers:

- Vertical Total Latch
- Vertical End Sync Latch

- Vertical Start Blank Latch
- Vertical End Blank Latch
- Vertical Counter

The Vertical latches are user programmable and may also be read by the host. The Vertical total latch determine the number of scan lines per field in interlaced mode and the number of lines per frame in non-interlaced mode. The Vertical end sync latch determines which line Vertical sync will end. The vertical start and end blank latches determine where vertical blank will start and end. The start and end values may be set equal to each other in which case, vertical start blank will determine the start of display updates but  $\sim$ CBLNK will contain NO vertical blanks. The Vertical counter counts the number of half lines in interlaced mode and the number of full lines in non-interlaced mode. This counter is read only by the host. Reading this counter may be useful but keep in mind that this counter runs asynchronous to SYSCLK and may need to be read several times in succession to guarantee the correct return value. The Vertical timing controller also synchronizes the Vertical timing signals to an external Vertical reset pulse.

The Vertical interrupt controller sets the vertical interrupt bit in the status register when the vertical counter reaches the line number value programmed into the Vertical interrupt latch. This latch is host programmable as well as readable by the host. NOTE that if the Vertical interrupt register is programmed with the value in the Vertical total register in interlaced mode, a Vertical interrupt will occur only once a FRAME at Vertical reset time.

### 3.6 DISPLAY UPDATE GENERATOR

The display update generator (DUGEN) is responsible for automatically creating memory read transfers in order to update a monitor with video information or automatically creating memory write transfers in order to acquire an image into video memory. The display update generator also contains the auto-acquire circuitry for host independent frame acquisitions. When the  $\sim$ ACQTRG pin is toggled low, the auto-acquire state machine waits for the beginning of a new frame, allows the DUGEN to acquire/display that frame, disables the DUGEN and sets the end-acquire bit in the status register. The  $\sim$ ACQTRG pin must remain low for continuous display to a monitor. The DUGEN may also be shut off by setting bit 13 of control register B. When the DUGEN is turned off in this manner, display updates immediately terminate and the DUGEN remains in its current state. The DUGEN may be programmed for display or acquire by programming bit 12 of control register B with the correct value. Display updates may be programmed to occur after every display line, every other, every fourth or every eighth display line by programming the Line Count Limit bits 8 and 9 of control register B with the correct value. One of four each of the row and column address strobes may be selected by the display update address register (DAR) or all four of each of the row and/or column strobes may be selected by programming the display update RAS/CAS OVerride bits 10 and 11 of control register B. NOTE that the row and column select bits of the DAR as well as row and column address bits 9 of the DAR are static i.e. not part of the display update address generation. The DUGEN provides address linearization called Reformat. Display update address reformat is necessary when interlaced data has been acquired into VRAM through SAM in a "bank-by-four" memory architecture and is to be displayed NON-interlaced. Display update reformat may be invoked by setting bit 14 of control register B.

The DUGEN creates updates differently for acquire vs. display. At the beginning of an acquire, the DUGEN updates the DAR at vertical start blank of a new frame but does not perform a write transform cycle. After the end of vertical blank and at the beginning of each horizontal blank time determined by the line count limit, the DUGEN performs a write transfer cycle (after the arbiter acknowledges the internal display update request) followed by DAR update. At the beginning of vertical blank of the end of the frame, the DUGEN completes one last write transfer cycle without a DAR update. The case for display is similar but performs both a DAR update and a read transfer cycle (in that order) at the beginning of a frame and for each successive line count limit reached.

The DUGEN contains three host accessible registers:

**DSR-** The twenty four bit Display Start Register consists of a twelve bit ROW address portion and a twelve bit COL address portion. This register determines where in memory the displayed (acquired) image will start. Adjusting the ROW portion of this register allows the user to SCROLL the image. Adjusting the COL portion of this register allows the user to PAN the image.

**DAR-** The twenty four bit Display Address Register is loaded with the contents of the DSR at the beginning of a frame. After each successive Line Count Limit has been reached, the contents of the Display Update Register (DUR) is added to the DAR. If the display is interlaced, one half of the value in the DUR is added to the DSR and the sum is placed in the DAR at the beginning of the second field.

**DUR-** The four bit Display Update Register determines the display update increment size and is intended to be programmed with the values of 1, 2, 4 or 8.

## 4. PROGRAMMABLE REGISTERS

This section describes the use of the ISC's programmable registers. The ISC contains eighteen programmable registers, one read only status register and three read only counters. The length of these registers vary in size from four to sixteen bits and are all host accessible through an eight bit data path a byte at a time.

The host processor accesses these registers via the internal register read/write cycles. These cycles are designed to look very much like memory cycles to the host. An internal register access is not allowed when the ISC is busy with an internally generated memory cycle. A function select code of 0 or 2 along with  $\sim$ RAE going low starts an internal register access. The  $\sim$ W signal determines the direction of the access and column address input pins 0 through 5 determine the register address. Column address bit 0 determines whether the high or low byte of the register is accessed. The input signal  $\sim$ CAE latches the register address. During a register write cycle, register data is accepted on Host Data (HD) pins 0 through 7. Since there is no data latch, setup and hold times must be observed.

In the following register descriptions, the following conventions are observed: The LSB of a register is the right most bit and conversely, the MSB of a register is the left most bit. Active bits in a register are represented with a capital 'A' and bits not implemented in a register are represented with a capital 'X'.

INPUT PIN VALUE	REGISTER NAME		
C C C C C	UPPER	LOWER	
A A A A A	BYTE	BYTE	
5 4 3 2 1	CA0=1	CA0=0	
0 0 0 0 0	XXXXAAAA	AAAAA	HORIZONTAL TOTAL
0 0 0 0 1	XXXXAAAA	AAAAA	HORIZONTAL END SYNC
0 0 0 1 0	XXXXAAAA	AAAAA	HORIZONTAL START BLANK
0 0 0 1 1	XXXXAAAA	AAAAA	HORIZONTAL END BLANK
0 0 1 0 0	XXXXAAAA	AAAAA	VERTICAL TOTAL
0 0 1 0 1	XXXXAAAA	AAAAA	VERTICAL END SYNC
0 0 1 1 0	XXXXAAAA	AAAAA	VERTICAL START BLANK
0 0 1 1 1	XXXXAAAA	AAAAA	VERTICAL END BLANK
0 1 0 0 0	XXXXAAAA	AAAAA	HORIZONTAL COUNTER *
0 1 0 0 1	XXXXAAAA	AAAAA	CSYNC COUNTER *
0 1 0 1 0	XXXXAAAA	AAAAA	VERTICAL COUNTER *
0 1 0 1 1	XXXXAAAA	AAAAA	VERTICAL INTERRUPT
0 1 1 0 0	AAAAA	AAAAA	CONTROL REGISTER A
0 1 1 0 1	AAAAA	AAAAA	CONTROL REGISTER B
0 1 1 1 0	AAAAA	AAAAA	X-Y ADDRESS REGISTER
0 1 1 1 1	XXXXXXX	AAAAA	BLOCK ADDRESS REGISTER
1 0 0 0 0	XXXXAAAA	AAAAA	DISPLAY START REG -COL
1 0 0 0 1	XXXXAAAA	AAAAA	DISPLAY START REG -ROW
1 0 0 1 0	XXXXAAAA	AAAAA	DISPLAY ADDRESS REG -COL
1 0 0 1 1	XXXXAAAA	AAAAA	DISPLAY ADDRESS REG -ROW
1 0 1 0 0	XXXXXXX	XXXXAAAA	DISPLAY UPDATE REGISTER
1 0 1 0 1	XXXXXXX	XXXXAAAA	STATUS REGISTER

TABLE 4-1 REGISTER ADDRESS MAP

\* =READ ONLY REGISTER



## 4.1 REGISTER VALUES AFTER RESET

At reset, the internal registers are set to values indicated in Table 4-2.

REGISTER NAME	VALUE AFTER RESET
HORIZONTAL TOTAL	XXXX 0010 0000 0000
HORIZONTAL END SYNC	XXXX 0000 1000 0000
HORIZONTAL START BLANK	XXXX 0010 0000 0000
HORIZONTAL END BLANK	XXXX 0000 1000 0000
VERTICAL TOTAL	XXXX 0010 0000 0000
VERTICAL END SYNC	XXXX 0000 1000 0000
VERTICAL START BLANK	XXXX 0010 0000 0000
VERTICAL END BLANK	XXXX 0000 1000 0000
HORIZONTAL COUNTER	XXXX 0000 0000 0000
CSYNC COUNTER	XXXX 0000 0000 0000
VERTICAL COUNTER	XXXX 0000 0000 0000
VERTICAL INTERRUPT	XXXX 0000 1000 0000
CONTROL REGISTER A	0000 0011 0000 0000
CONTROL REGISTER B	0000 0011 0000 0000
X-Y ADDRESS REGISTER	0000 0000 0000 0000
BLOCK ADDRESS REGISTER	XXXX XXXX 0000 0000
DISPLAY START REG -COL	XXXX 0000 0000 0000
DISPLAY START REG -ROW	XXXX 0000 0000 0000
DISPLAY ADDRESS REG -COL	XXXX 0000 0000 0000
DISPLAY ADDRESS REG -ROW	XXXX 0000 0000 0000
DISPLAY UPDATE REGISTER	XXXX XXXX XXXX 0000
STATUS REGISTER	XXXX XXXX XXXX 0000

TABLE 4-2 INTERNAL REGISTER VALUES AFTER RESET

Note that the default refresh burst length is eight, the default number of wait states is zero, the default line count limit is eight and the default memory size is 256K. Also, the screen is disabled by default.

## 4.2 HOST INTERFACE REGISTERS

The ISC contains two, host programmable, sixteen bit control registers that determine the behavior of display timing, display update addressing, X-Y addressing, host interface signals, memory control and interface signals, DRAM refresh and interrupt control. There is also a four bit read-only status register that the host may access.

## 4.2.1 CONTROL REGISTER A

B15	B14	B13	B12	B11	B10	B9-B8	B7-B6	B5-B3	B2-B0
MEM SIZE	AG RE-FRMT	XRAS MODE	XCAS MODE	AG RAS OVRD	AG CAS OVRD	REFRSH BURST LENGTH	WAIT STATE LIMIT	X-Y ROW STPSZ	X-Y COL STPSZ

FIGURE 4-1

### BITS FUNCTION

#### B2-B0 X-Y COLUMN STEP SIZE

These three bits control how much the column address counter will be incremented or decremented during X-Y addressing mode. The column address counter is architected such that the two LSBs of the column address register control the four column address strobes. With bit B2=0, bits B1-B0 set the column address register step size to 1, 2, 4 or 8. With bit B2=1, bits B1-B0 set the column address register step size to 4, 8, 16 or 32 (ie the column address strobes will not be affected).

#### B5-B3 X-Y ROW STEP SIZE

These three bits control how much the row address counter will be incremented or decremented during X-Y addressing mode. The row address counter is architected such that the two LSBs of the row address register control the four row address strobes. With bit B5=0, bits B4-B3 set the row address register step size to 1, 2, 4 or 8. With bit B5=1, bits B4-B3 set the row address register step size to 4, 8, 16 or 32 (ie the row address strobes will not be affected).

B2	B1	B0	STARTING ADDRESS BIT AFFECTED	B5	B4	B3	STARTING ADDRESS BIT AFFECTED
0	0	0	CS0 -COL SEL BIT 0	0	0	0	RS0 -ROW SEL BIT 0
0	0	1	CS1 -COL SEL BIT 1	0	0	1	RS1 -ROW SEL BIT 1
0	1	0	CA0 -COL ADD BIT 0	0	1	0	RA0 -ROW ADD BIT 0
0	1	1	CA1 -COL ADD BIT 1	0	1	1	RA1 -ROW ADD BIT 1
1	0	0	CA0 -COL ADD BIT 0	1	0	0	CA8/7 -COL ADD MSB
1	0	1	CA1 -COL ADD BIT 1	1	0	1	RA0 -ROW ADD BIT 0
1	1	0	CA2 -COL ADD BIT 2	1	1	0	RA1 -ROW ADD BIT 1
1	1	1	CA3 -COL ADD BIT 3	1	1	1	RA2 -ROW ADD BIT 2

TABLE 4-3 STEPSIZE CONTROL

#### B7-B6 WAIT STATE LIMIT

These two bits determine the number of wait states inserted into host initiated cycles. A wait state is a delay of one-half of a SYSCLK period inserted into a cycle to increase its duration. Zero through three wait states are available.

B7	B6	# OF WAIT STATES
0	0	0 WAIT STATES
0	1	1 WAIT STATE
1	0	2 WAIT STATES
1	1	3 WAIT STATES

TABLE 4-4 WAIT STATE LIMIT

**B9-B8 REFRESH BURST LENGTH**

Bits B9-B8 contain a two bit encoded number specifying the number of DRAM refresh cycles to be generated per horizontal scan line. The number of refresh cycles per scan line allowed are 0, 2, 4 or 8.

B9	B8	REFRESH BURST LENGTH
0	0	NO REFRESH CYCLES
0	1	2 REFRESH CYCLES
1	0	4 REFRESH CYCLES
1	1	8 REFRESH CYCLES

TABLE 4-5 REFRESH BURST LENGTH

**B10 ADDRESS GENERATOR CAS OVERRIDE**

When this bit is set to a one, all four  $\sim$ CAS lines are forced to their active-low level during the following types of cycles: HOST DIRECT, X-Y INDIRECT, REAL-TIME and HOST INITIATED SHIFT-REGISTER TRANSFER.

\* WARNING: Depending on the memory architecture, CAS override during a READ cycle could result in data collision.

**B11 ADDRESS GENERATOR RAS OVERRIDE**

When this bit is set to a one, all four  $\sim$ RAS lines are forced to their active-low level during the following types of cycles: HOST DIRECT, X-Y INDIRECT, REAL-TIME and HOST INITIATED SHIFT-REGISTER TRANSFER.

\* WARNING: Depending on the memory architecture, RAS override during a READ cycle could result in data collision.

**B12 EXTERNAL CAS MODE**

When this bit is set to a one, the input value at pins S1 and S0 replace the two-bit value at locations B1-B0 of the BLOCK address register and determine which of the four  $\sim$ CAS outputs is driven low during a non block-mode host-direct or shift-register transfer cycle.

**B13 EXTERNAL RAS MODE**

When this bit is set to a one, the input value at pins S1 and S0 replace the two-bit value at locations B5-B4 of the BLOCK address register and determine which of the four  $\sim$ RAS outputs is driven low during a non block-mode host-direct or shift-register transfer cycle.

\* NOTE: S1-S0 are latched on  $\sim$ CAE

**B14 ADDRESS GENERATOR REFORMAT**

When this bit is set to one, an interlaced image that was captured as two video lines per memory row will appear to be in non-interlaced format during host initiated memory cycles. REFORMAT is memory size sensitive so B15 of control register A must be set to the correct value. REFORMAT works by swapping ROW bit 0 with COL bit 7 using 256K VRAM or with COL bit 8 using 1M VRAM.

\* NOTE: Be careful when using fast page mode with REFORMAT!

**B15 MEMORY SIZE**

This bit sets the memory size for correct display updates and reformat control. B15=0 sets the memory size for 256K VRAM, B15=1 sets the memory size for 1M VRAM.

**CONTROL REGISTER B**

B15	B14	B13	B12	B11	B10	B9-B8	B7	B6	B5	B4	B3	B2	B1	B0
BLOCK MODE ENABLE	DU REFRMT	DU INHBT	DU DIR	DU RAS OVRD	DU CAS OVRD	LINE COUNT LIMIT	ENDACQ INT ENABLE	ERROR INT ENABLE	VERT INT ENABLE	INTL ENABLE	VIDS TD	EXT HSYNC ENABLE	EXT VSYNC ENABLE	SCREEN ENABLE

**FIGURE 4-2****BITS FUNCTION****B0 SCREEN ENABLE**

When this bit is zero, the  $\sim$ CBLANK pin is driven low continuously. When B0 is set to one, the  $\sim$ CBLANK pin is driven low only during horizontal and vertical blanking times.

**B1 EXTERNAL VSYNC ENABLE**

When B1=0, the ISC generates the vertical sync and vertical reset signals internally ( $\sim$ VSYNC and  $\sim$ VRST pins respectively) and ignores any signal present at the  $\sim$ XVRST input pin. When B1=1, the external VRST mode is enabled and the ISC locks onto the externally-generated vertical reset signal ( $\sim$ XVRST pin). The signals at the  $\sim$ VSYNC and  $\sim$ VRST output pins in external VRST mode are essentially delayed versions of their externally generated counterparts except for the duration of VSYNC which is still dependent on the programmed value of the VESYNC register.

\* NOTE: When external VRST is enabled, serrated pulses are not generated and  $\sim$ CSYNC simply becomes another  $\sim$ HSYNC.

**B2 EXTERNAL HSYNC ENABLE**

When B2=0, the ISC generates the horizontal sync signal internally ( $\sim$ HSYNC pin) and ignores any signal present at the  $\sim$ XHSYNC input pin. When B2=1 the external HSYNC mode is enabled and the ISC locks on to the externally-generated horizontal sync signal ( $\sim$ XHSYNC pin). The signal at the  $\sim$ HSYNC output pin in external HSYNC mode is essentially a delayed version of its externally generated counterpart except for the duration of HSYNC which is still dependent on the programmed value of the HESYNC register.

**B3 VIDEO STANDARD**

When B3=0, the composite sync signal follows the NTSC TV standard and when B3=1, the composite sync signal follows the PAL TV standard, if interlaced is enabled.

**B4 INTERLACE ENABLE**

When B4=0, the ISC is configured for non-interlaced scan and  $\sim$ CSYNC becomes another  $\sim$ HSYNC. When B4=1, the ISC is configured for interlaced scan and composite sync is generated according to the

TV standard selected.

**B5 VERTICAL INTERRUPT ENABLE**

When B5=0, the setting of the vertical interrupt flag in the status register does not cause an interrupt to the host processor. When B5=1, the interrupt request is enabled.

**B6 ERROR INTERRUPT ENABLE**

When B6=0, the setting of an error interrupt flag in the status register does not cause an interrupt to the host processor. When B6=1, the setting of either an display or refresh error interrupt flag causes an interrupt request.

**B7 END-ACQUIRE INTERRUPT ENABLE**

When B7=0, the setting of the end-of-acquire interrupt flag in the status register does not cause an interrupt to the host processor. When B7=1, the interrupt is enabled.

**B9-B8 LINE COUNT LIMIT**

The Line Count Limit determines the number of horizontal lines that are counted by the scan line counter before a display update cycle is granted. Possible limits are: every line, every other line, every fourth line and every eighth line. The scan line counter repeatedly counts from zero to the scan line limit, incrementing at the beginning of every COMPOSITE blank interval. The scan line counter is reset at the beginning of every vertical blank period and remains inactive during vertical blank. When the scan line limit is reached and an internal display update is requested. When the arbiter grants a display update acknowledge, the display update request is removed and the scan line counter is reset. The display address register is updated BEFORE the display update cycle in DISPLAY mode and AFTER the display update cycle in ACQUIRE mode. When the line scan limit is set to zero, display updates occur on every scan line.

B9	B8	LINE COUNT LIMIT
0	0	AFTER EACH SCAN LINE
0	1	EVERY OTHER SCAN LINE
1	0	EVERY 4TH SCAN LINE
1	1	EVERY 8TH SCAN LINE

**TABLE 4-6 DISPLAY UPDATE CONTROL**

**B10 DISPLAY UPDATE CAS OVERRIDE**

When B10=1, all four COL address strobe pins are active during a display update cycle. When B10=0, only one of four strobes is active during a display update cycle and the active strobe is selected by the value contained in bits B11-B10 of the display address register.

**B11 DISPLAY UPDATE RAS OVERRIDE**

When B11=1, all four ROW address strobe pins are active during a display update cycle. When B11=0, only one of four strobes is active during a display update cycle and the active strobe is selected by the value contained in bits B23-B22 of the display address register.

**B12 DISPLAY UPDATE DIRECTION**

When B12=0, the ISC is in Display mode and display update cycles transfer data from the memory cell array to the shift register. When B12=1, the ISC is in Acquire mode and "display" update cycles transfer data from the shift register to the memory cell array.

- B13 DISPLAY UPDATE INHIBIT**  
When this bit is set to a one, display update cycles are inhibited.
- B14 DISPLAY UPDATE REFORMAT**  
When this bit is set to one, an interlaced image that was captured as two video lines per memory row will be addressed in non-interlaced format during display update cycles. REFORMAT is memory size sensitive so B15 of control register A must be set to the correct value. REFORMAT works by swapping ROW bit 0 with COL bit 7 using 256K VRAM or with COL bit 8 using 1M VRAM.
- B15 BLOCK MODE**  
Block Mode addressing is available when the ISC is used in systems with limited address space. By setting B15=1 and programming the block address register with the two MSBs of each of the ROW and COLUMN addresses and the two bits each of the ROW and COLUMN select bits, memory can be accessed in 64K blocks using the eight LSBs of each of the ROW and COLUMN address pins.  
\* NOTE: The Block Address register is part of the ROW and COLUMN address registers in the address generator and is subject to change value during X-Y addressing mode.

**STATUS REGISTER**

B3	B2	B1	B0
END ACQUIRE	REFRESH ERROR	DISPLAY ERROR	VERTICAL INTERRUPT

**FIGURE 4-3**

The status register contains four bits, each representing a particular internal condition. When one of the bits is set and the corresponding interrupt-enable bit in Control Register B is set to one, the ISC sends an interrupt request to the host processor by driving the ~INT pin to its active low level. The status register can be read, but not written to, by the host processor. A read of the status register by the host will cause all of the bits to be reset to zero, thereby clearing the interrupt request.

- BITS      FUNCTION**
- B0      VERTICAL INTERRUPT**  
A one in this bit indicates that the vertical counter has reached the value programmed in the Vertical Interrupt Register.
- B1      DISPLAY ERROR**  
A one in this bit indicates that a display update cycle was unable to be performed during the composite blanking period.
- B2      REFRESH ERROR**  
A one in this bit indicates that the ISC was unable to execute the designated number of cycles before the end of the horizontal blanking period.

### **B3 END ACQUIRE INTERRUPT**

A one in this bit indicates the end of a frame(s) of acquiring (or displaying) data if the ~ACQTRG pin was triggered.

## **4.3 ACQUIRE/DISPLAY CONTROL REGISTERS**

### **4.3.1 DISPLAY ADDRESS REGISTER**

The twenty four bit display address register (DAR) consists of a twelve bit ROW portion and a twelve bit COL address portion. This register contains the address to be output during the next automatic display update cycle. In general, this register is updated once at the beginning of each vertical blank and at the beginning of a horizontal blank period when the line scan limit has been reached. During a frame ACQUIRE, the DAR is updated once at the beginning of vertical blank at the beginning of a frame then, a memory transfer cycle with a DAR update occur at every scheduled update time. For the last update of a frame at vertical blank time, only a memory transfer occurs to acquire the very last line of data. During a frame DISPLAY, the DAR is updated then a memory transfer cycle occurs at the beginning of a frame at vertical blank time and at every scheduled display update cycle. No update is performed for the last vertical blank of a single frame. The DAR also provides the ROW portion of the address for REAL-TIME processing mode. Display address bits RA9, CA9, RS1, RS0, CS1, CS0 and CA0 through CA8 of are not part of the normal update cycles. These bits merely mimic what's in the display start register at these locations.

The host may access this register in two ways. One is by performing successive read cycles to insure the integrity of the returned data. The other is by using the vertical interrupt register to get you to the end of a line, then wait through the horizontal blank time before performing an access.

### **4.3.2 DISPLAY START REGISTER**

The twenty four display start register (DSR) consists of a twelve bit ROW address portion and a twelve bit COL address portion. This register determines where in memory the displayed (acquired) image will start. The contents of this register are loaded into the DAR at the beginning of VERTICAL blank when in non-interlaced mode and at the beginning of VERTICAL blank at the beginning of a frame when in interlaced mode. Adjusting the ROW portion of this register allows the user to SCROLL the image. Adjusting the COL portion of this register allows the user to PAN the image. This register may be both written to and read from by the host.

### **4.3.3 DISPLAY UPDATE REGISTER**

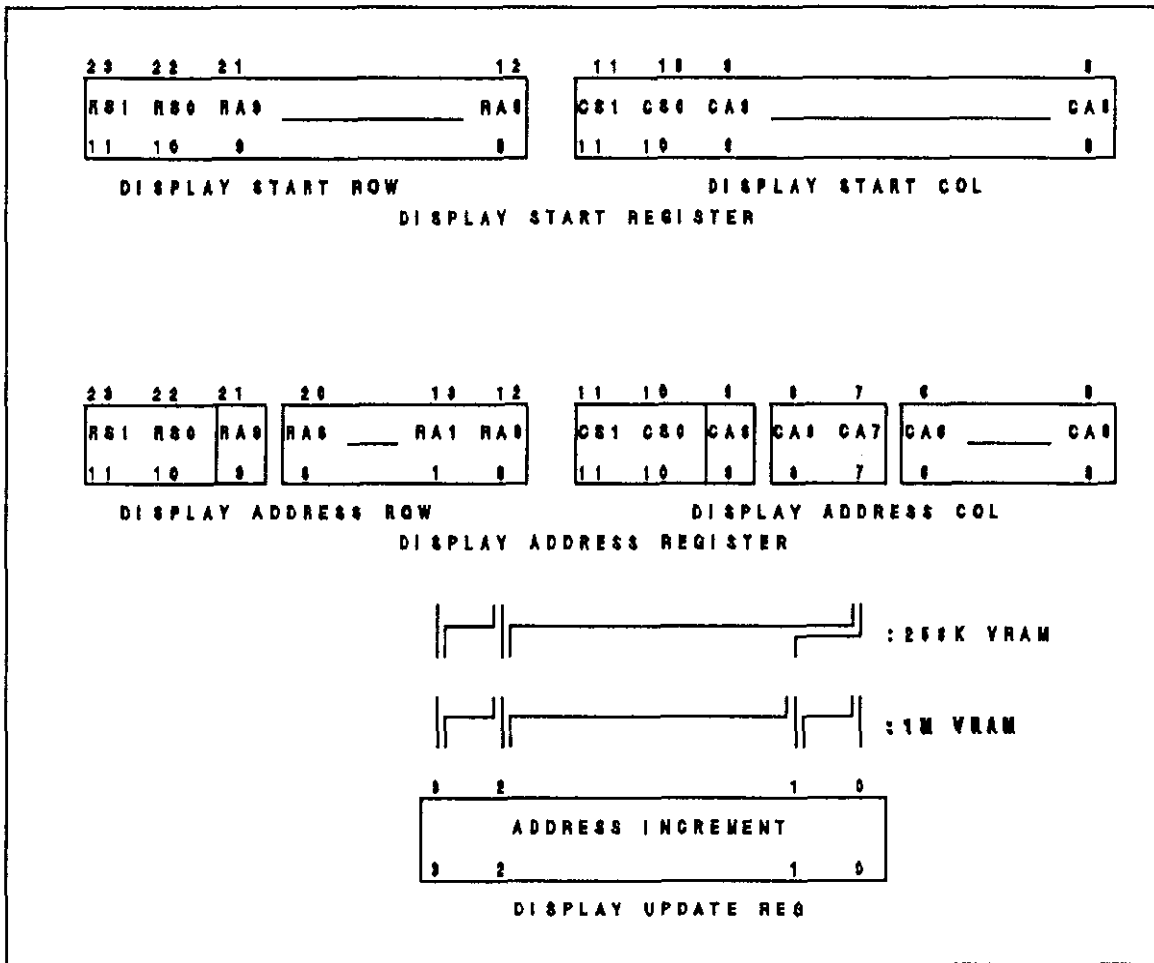
The four bit display update register (DUR) contains the value by which the display address is incremented. Valid increment values are 0, 1, 2, 4 and 8. This register may be written to or read by the host.

#### *NON-INTERLACED MODE OPERATION*

During a scheduled DAR update at the beginning of HORIZONTAL blank, the contents of the display update register (DUR) are added to the display address register (DAR).

#### *INTERLACED MODE OF OPERATION*

During a scheduled DAR update at the beginning of HORIZONTAL blank, the contents of the display update register (DUR) are added to the display address register (DAR). At the start of VERTICAL blank preceding an EVEN field (ie mid-frame), one-half the value contained in the DUR is added with the value from the DSR and the result stored in the DAR. This allows the offset needed to display/acquire two video fields.



#### 4.4 VIDEO TIMING REGISTERS

The Display Timing Generator (DTGEN) creates all of the signals necessary to operate a CRT display in either non-interlaced or interlaced NTSC or PAL standards. In addition, the DTGEN can sync to an external video timing source such as external video or another ISC. When synchronized to external VRST, the DTGEN provides HSYNC to be phase lock looped to an external HSYNC to create a stable video clock for a tightly coupled system. The DTGEN also creates a vertical interrupt signal at a user programmed interval.

NAME	DESCRIPTION
HCNTR	The horizontal counter is a 12 bit counter that counts video clocks until reset by the horizontal total strobe that is internally generated when the HCNTR reaches the value stored in the horizontal total register. The HCNTR is used in the creation of HSYNC, HBLANK and the internally generated half line strobe.
CCNTR	The composite counter is a 12 bit counter that counts video clocks until reset by either the horizontal total strobe or the half line strobe and is used in the creation of the equalizing and broad pulses for composite sync.



VCNTR	The vertical counter is a 13 bit counter that counts horizontal lines in non-interlaced mode and half lines in interlaced mode until reset by the vertical total strobe that is internally generated when the VCNTR reaches the value programmed in the VTOTAL register. It is used in the creation of VSYNC, VBLANK and CSYNC.
HTOTAL	The horizontal total register is a 12 bit user programmable register and determines the length of a horizontal line (in video clock units).
HESYNC	The horizontal end sync register is a 12 bit user programmable register and determines the width of the horizontal sync pulse (in video clock units).
HSBLANK	The horizontal start blank register is a 12 bit user programmable register and determines where in a line horizontal blank begins(in video clock units).
HEBLANK	The horizontal end blank register is a 12 bit user programmable register and determines the width of the horizontal blank pulse (in video clock units).
VTOTAL	The vertical total register is a 12 bit user programmable register and determines the length of a field/frame (in horizontal lines).
VESYNC	The vertical end sync register is a 12 bit user programmable register and determines the width of the vertical sync pulse (in horizontal lines).
VSBLANK	The vertical start blank register is 12 bit user programmable register and determines where the vertical blank begins (in horizontal lines).
VEBLANK	The vertical end blank register is a 12 bit user programmable register and determines the width of vertical blank (in horizontal lines).
VINT	The vertical interrupt register is a 12 bit user programmable register and determines where in a field/frame a vertical interrupt will occur (in horizontal lines). An interrupt will occur once a FRAME in non-interlaced mode and once a FIELD in interlaced mode with the exception of when the value in the VINT register is set equal to the value in the VTOTAL register. In this case, an interrupt will occur once each FRAME.

#### 4.4.1 VIDEO TIMING RELATIONSHIPS TO DTGEN REGISTERS

##### DTGEN REGISTERS

$$HTOTAL = [\text{Horizontal line time} / \text{VCLK period}] - 1$$

$$HESYNC = [\text{Horizontal sync time} / \text{VCLK period}] - 1$$

$$HSBLANK = HTOTAL - [\text{Hfront porch} / \text{VCLK period}]$$

$$HEBLANK = [(\text{Hsync time} + \text{Hback porch}) / \text{VCLK period}] - 1$$

$$VTOTAL(\text{non-interlaced}) = \# \text{Hlines per frame} - 1$$

$$VTOTAL(\text{interlaced}) = [\# \text{Hlines per frame} - 1] / 2$$

$$VESYNC = \text{Vsync width} - 1 \text{ (in } \# \text{ Hlines)}$$

VSBLANK = VTOTAL-Vfront porch width (in #Hlines)

VEBLANK = Vsync width + Vback porch-1 (in #Hlines)

VINT = line # interrupt is to occur

\*NOTE: The following restrictions apply when programming the internal DTGEN registers for video use:

HTOTAL>HESYNC	HTOTAL=>HSBLANK
HTOTAL=>HEBLANK	HSBLANK<>HEBLANK
VTOTAL>VESYNC	VTOTAL=>VSBLANK (non-int)
VTOTAL=>VEBLANK	VTOTAL>VSBLANK (int)

#### 4.5 ADDRESS GENERATOR

The X-Y addressing mode allows access to all of DRAM with only a four bit code. This is a very useful feature for systems that are register mapped or have limited memory address space. A memory read or write access that utilizes the contents of the X-Y address pointer for the memory address is called an X-Y indirect cycle.

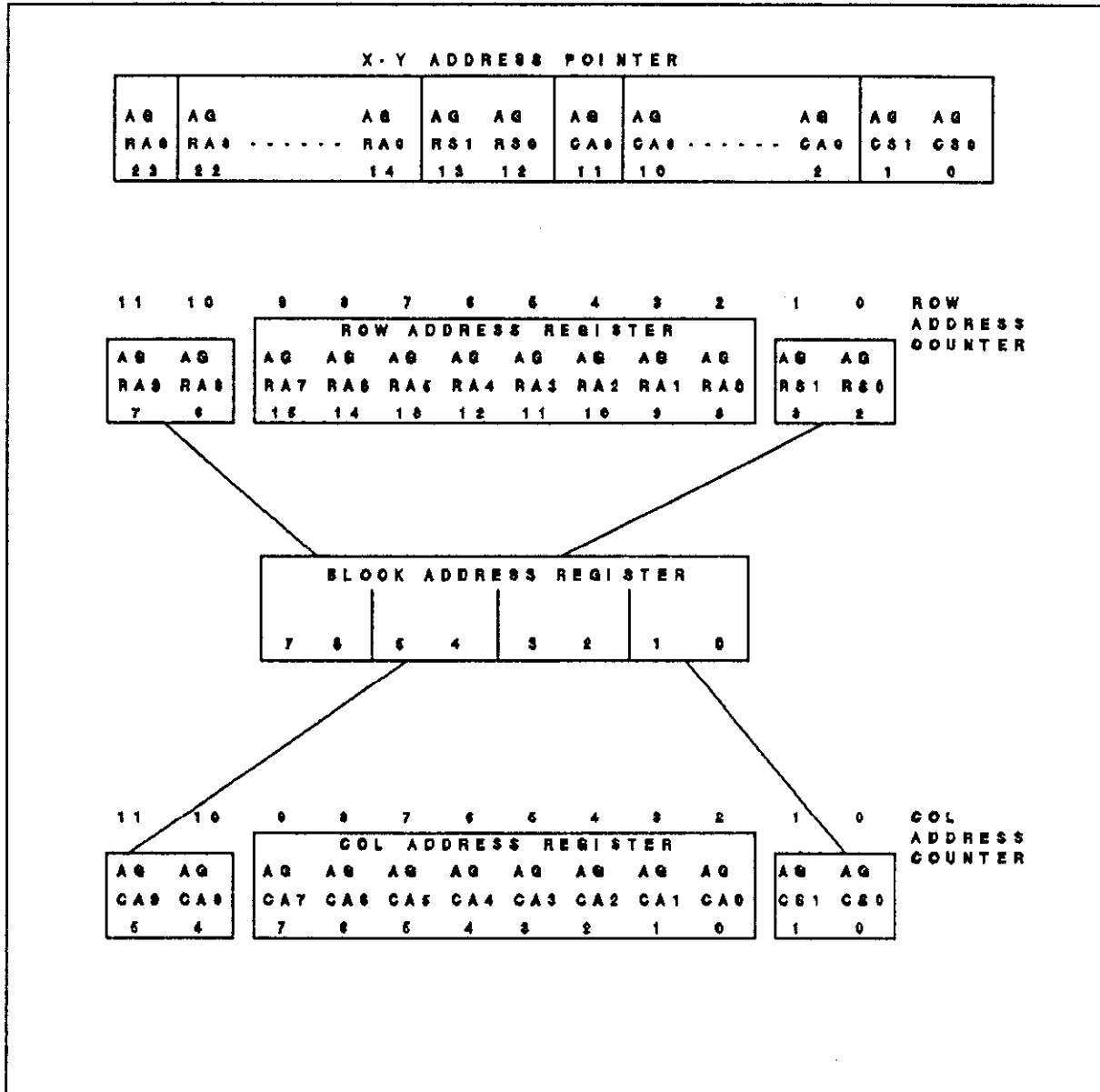
The X-Y addressing mode is enabled with a Function Select code of one (FS2-FS0 = 001). The 4-bit adjustment code on input CA3 - CA0 during an X-Y indirect cycle determines the manner in which the contents of the ROW and COL address counters are updated following the completion of the X-Y indirect cycle, as indicated in Table 4-7. The X-Y adjustment code is latched on the falling edge of ~CAE. The COL address counter performs an address update on the rising edge of ~CAE and the ROW address counter performs an update on the rising edge of ~RAE. At the end of an X-Y indirect cycle, both ~CAE and ~RAE must go high within the same SYSCLK period. This is to insure that a COL-to-ROW carry is recognized if one had been generated. The X-Y adjustment size is determined by the ROW STEPSIZE (control register A, bits 5-3) and the COL STEPSIZE (control register A, bits 2-0) as in Table 4-3.

CA3	CA2	CA1	CA0	X-Y FUNCTION	ADJUST
0	0	0	0	NOP	NOP
0	0	0	1	+X	NOP
0	0	1	0	-X	NOP
0	0	1	1	CLR X	NOP
0	1	0	0	NOP	+Y
0	1	0	1	+X	+Y
0	1	1	0	-X	+Y
0	1	1	1	CLR X	+Y
1	0	0	0	NOP	-Y
1	0	0	1	+X	-Y
1	0	1	0	-X	-Y
1	0	1	1	CLR X	-Y
1	1	0	0	NOP	CLRY
1	1	0	1	+X	CLRY
1	1	1	0	-X	CLRY
1	1	1	1	CLR X	CLRY

TABLE 4-7

The address generator consists of a 24 bit address pointer which consists of a 12 bit ROW address counter and a 12 bit COLumn address counter. These counters are accessed by the host via 3, 8 bit register locations.

- COL ADDRESS REGISTER                    AGCA7 - AGCA0
- ROW ADDRESS REGISTER                AGRA7 - AGRA0
- BLOCK ADDRESS REGISTER            AGRA9,8 AGCA9,8 AGRS1,0 AGCS1,0



The X-Y address pointer is arranged such that the COL address counter creates the lower half of the pointer address and the ROW address counter creates the upper half of the pointer address. The column select bits make up the two LSB's of the COL address counter. The row select bits make up the two LSB's of the ROW address counter. Both ROW address bit 9 and COL address bit 9 are static and do not participate in the address count. These two bits are programmable, however, and are sent to Memory Address bit 9 during the appropriate RAS/CAS cycle times. The MSB of the COL address counter is either column address bit 7 (when the memory size bit is set to 0, control register A bit 15) or column address bit 8 (when the memory size bit is set to 1). When column bit 7 is the MSB of the COL address counter, then column address bit 8 becomes static

and does not participate in the address count. The MSB of the COL address counter carries over to the LSB of the ROW address counter. The ROW address counter carry-in position is determined by the MSB of ROW STEPSIZE (control register A, bit 5). When the ROW STEPSIZE MSB equals 0, the carry is to ROW address counter bit 0 (ie. row select bit 0). When the ROW STEPSIZE MSB equals 1, the carry is to ROW address counter bit 2 (ie. row address bit 0). For memory architectures that store two video lines per row of memory, the COL address register MSB can be used as the row address LSB. A ROW STEPSIZE = 4 (control register bits 5,4 and 3 = 100) will cause the column MSB to change on the rising edge of  $\sim$ CAE during an X-Y address cycle.

Programming the address pointer for an initial value is merely a matter of writing to the 3 address registers. The COL address register is simply the 8 LSB's of the column address. The ROW address register consists of the 8 LSB's of the row address. The BLOCK address register consists of the two MSB's each of the row address and the column address as well as the two row select bits and two column select bits. The BLOCK address register has a second function. In systems with limited address space, this register allows the user to move through memory in 64K blocks. By setting control register B, bit 15 to 1, the user may use address input pins CA7 - CA0 and RA7 - RA0 to move within a 64K block determined by the contents of the BLOCK address register. Note that since the BLOCK address register is part of the X-Y address pointer, its contents are subject to change after an X-Y cycle is performed.

For memory architectures that store two video lines of data per row of memory in interlaced format (ie. data is in memory as Line# 1,3,2,4,5,7,6,8,etc.) the ISC can linearize a memory access by setting the AGREFORMAT bit to 1 (control register A bit 4). Data will then be accessed from memory as Line# 1,2,3,4,5,6,7,8,etc. The ISC performs this function by swapping the column MSB with row bit 0 during memory addressing time. Remember, the column MSB selection is memory size dependent.

The chip also provides the ability for fast page mode memory access. The chip provides this feature by allowing the  $\sim$ CAE input pin a direct path to  $\sim$ CAS outputs once the initial setup of the memory is complete. The user must hold  $\sim$ RAE low for the duration of the cycle and toggle  $\sim$ CAE for each new column update. The user must obey memory precharge requirements and all other memory specific timing associated with this mode. The ISC does not detect row changes and so the user must provide this function so that row boundaries are not crossed during a fast page mode access. Fast page mode may be used with both memory direct and memory indirect cycles.

## 5. HOST AND MEMORY INTERFACE OPERATION

The ISC performs two types of access cycles; host initiated cycles and internally generated cycles. The five host initiated cycles include: Host Direct, X-Y Indirect, Shift-Register Transfer, Internal Register access and Real-Time access. These host initiated cycles are selected with the function select pins (FS2-FS0) and are initiated when  $\sim$ RAE goes low. The function select code is latched on the falling edge of  $\sim$ RAE. The two internally generated cycles are: Display/Acquire Update and Burst Refresh.

FS2	FS1	FS0	CYCLE
0	0	0	Register-access
0	0	1	X-Y Indirect
0	1	0	Register-access
0	1	1	Host-direct access
1	0	0	Write Transfer
1	0	1	Read Transfer
1	1	0	Real-Time access
1	1	1	Reserved

TABLE 5-1 FUNCTION SELECT DECODE

### 5.1 ARBITRATION

The arbiter that is built into the ISC controls the scheduling of the automatic display update cycle, the automatic burst refresh cycle and any host initiated cycle. When faced with a conflict, the arbiter grants requests according to the following priority:

- 1) Any cycle already in progress
- 2) A display/acquire update cycle (if enabled)
- 3) A DRAM burst refresh cycle(s) (if enabled)
- 4) A host initiated cycle (including internal register access)

Both display/acquire updates and DRAM refresh are requested at the beginning of horizontal blank. When both display/acquire updates and DRAM refresh are enabled, the arbiter allows the display/acquire update to occur first and then allows the DRAM burst refresh to proceed immediately following. If a display update was not allowed to occur by the end of horizontal blank, a display update error is generated in the status register. If a DRAM burst refresh was not allowed to occur or finish by the end of horizontal blank, a refresh error is generated in the status register.

### 5.2 INTERNAL REGISTER ACCESS

There are 22, 16 bit register locations in the ISC that are host accessible. Since the ISC's host data bus interface is only 8 bits wide, the internal registers are accessed as lower and higher bytes. An internal register access cycle is initiated with a function select code of 0 or 2 and the falling edge of  $\sim$ RAE. The direction of the transfer is determined by the  $\sim$ W input pin. Column address input pin 0 determines whether the lower or higher byte of the 16 bit register is accessed. Column address bits 1 through 5 selects one of the 22 register locations.

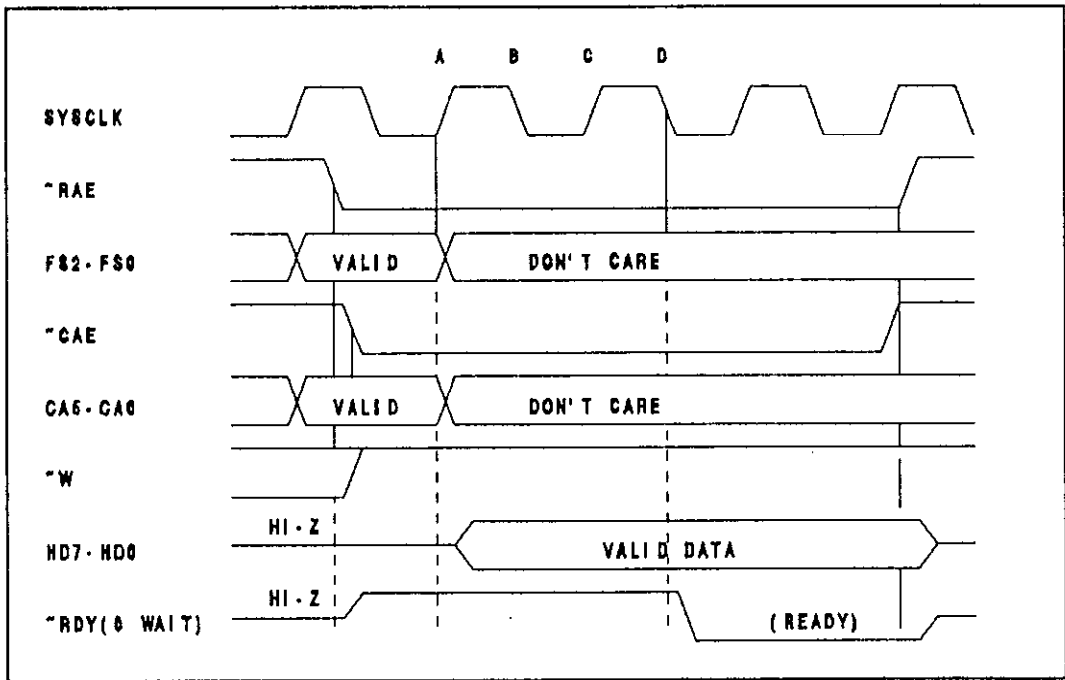


FIGURE 5-1 INTERNAL REGISTER READ ACCESS

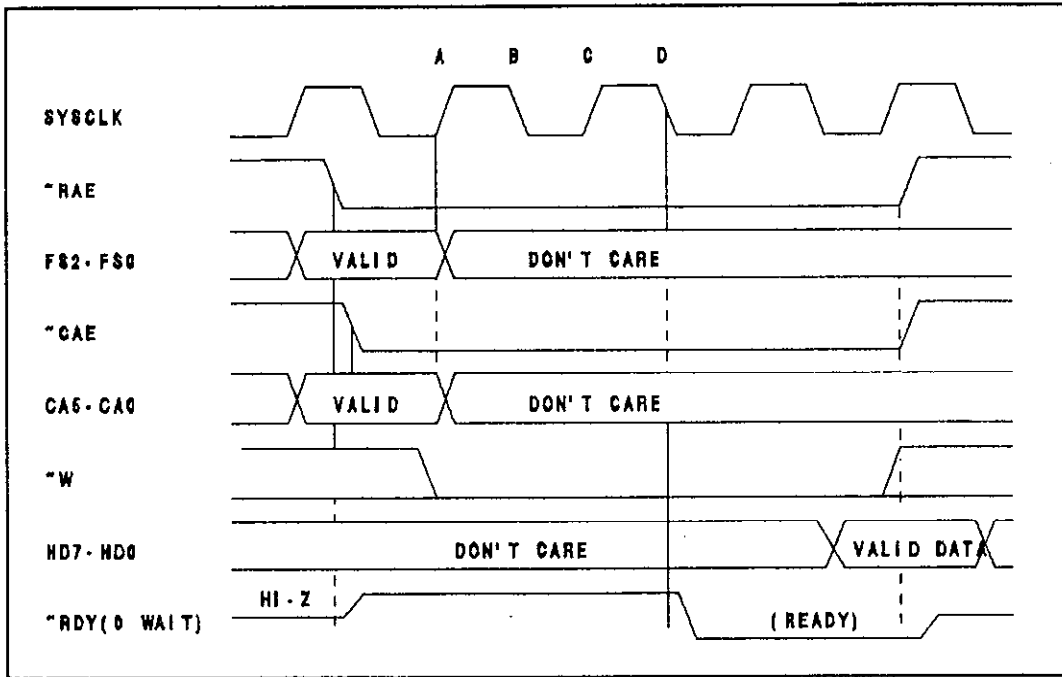


FIGURE 5-2 INTERNAL REGISTER WRITE ACCESS

Data bus pins HD7-HD0 are bidirectional and  $\sim W$  must be valid prior to clock edge 'A' of the register cycle or the enabling of external data buffers to prevent buffer conflict, which could damage the ISC. Since the ISC does not latch host input data, the user must ensure that host data remains valid past the rising edge of  $\sim CAE$  or  $\sim W$  at the end of a register write cycle. During a register read cycle, the  $\sim W$  input must remain valid for the duration of the cycle.

The timing of a register read cycle is shown in figure 5-1. By driving  $\sim RAE$  low, the host processor signals the start of a cycle. The FS2-FS0 signal inputs are latched on this edge of  $\sim RAE$ . The CA5-CA0 inputs are latched on the falling edge of  $\sim CAE$ . The  $\sim RDY$  pin transitions from the high impedance state to the active high "not ready" state. After the appropriate number of wait states have been counted out, the  $\sim RDY$  pin transitions to the active low "ready" state. At the end of the cycle, when  $\sim RAE$  transitions high, the  $\sim RDY$  pin goes back to the high impedance state. The ISC detects  $\sim RAE$  going low and begins the cycle on SYSCLK edge 'A' (assuming there are no conflicts with an internally generated cycle). Valid data is available just after clock edge 'A' and a 0 wait state, active low ready signal is asserted on clock edge 'D'.

The register write cycle of Figure 5-2 is similar to the register read cycle. Data to the ISC on pins HD7-HD0 must be valid before either  $\sim CAE$  or  $\sim W$  go high and must remain valid just after these signals going high.

### 5.3 DISPLAY UPDATE CYCLE

A display (acquire) update is performed automatically by the ISC. A display update is basically an automatically generated VRAM read transfer cycle in which the contents of a row of memory is transferred to the Serial Access Memory (SAM) register. An acquire update is similarly an automatically generated VRAM write transfer cycle in which the contents of SAM is transferred to a row of memory.

The contents of the row portion of the display address register determines which row in memory the transfer will occur. The contents of the column portion of the display address register determines the tap point for the transfer.

The ISC first creates an internal display update request. The arbiter determines if any other cycle is in progress. If all is clear, the arbiter creates an acknowledge to this request. The VRAM controller inside the ISC then begins the cycle on the rising SYSCLK edge 'A' by pointing to the row portion of the display address register and assertion  $\sim TROE$  low (also  $\sim MW$  low during an acquire). At clock edge 'B'  $\sim RAS$  is asserted. At clock edge 'C', the memory address points to the column portion of the display address register. At clock edge 'D',  $\sim CAS$  is asserted. At clock edge 'F',  $\sim TROE$  is brought back high. The cycle ends on clock edge 'G'. Once a display update cycle begins it takes three SYSCLK cycles to complete the cycle.

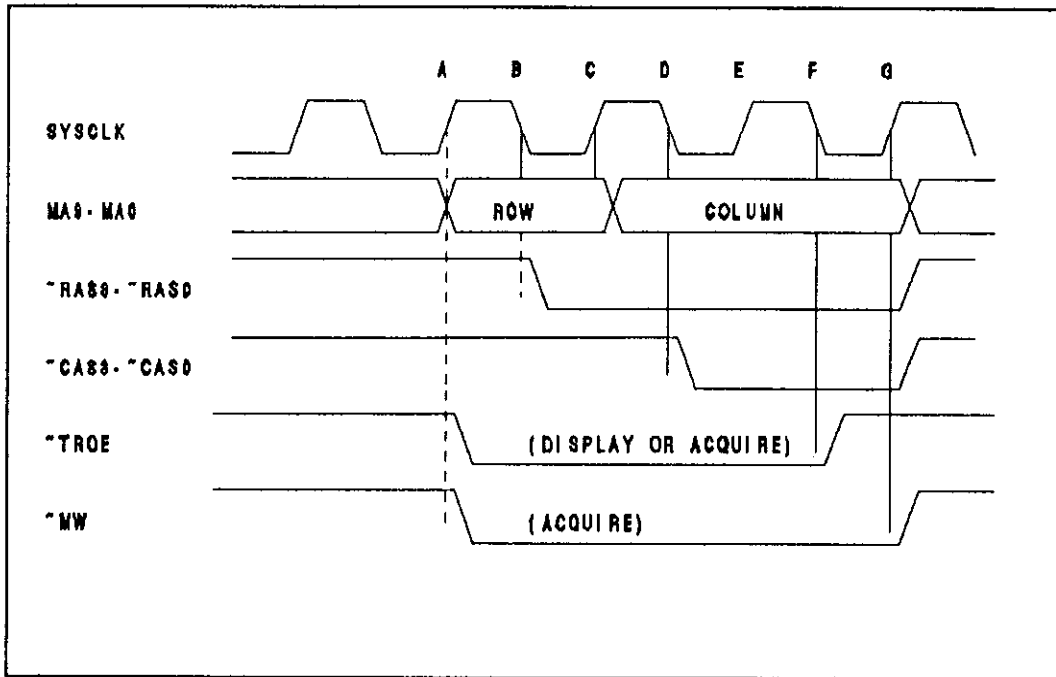


FIGURE 5-3 DISPLAY OR ACQUIRE UPDATE CYCLE

#### 5.4 CAS-BEFORE-RAS REFRESH CYCLE

At the beginning of each horizontal blank, an internal refresh request is generated if DRAM Refresh is enabled (control register A, bits 8 and 9). The arbiter then determines if a cycle is in progress or a display update cycle is scheduled. If other cycles are in progress or are pending, the arbiter holds off the refresh until the completion of these cycles, otherwise the arbiter sends a Refresh Acknowledge to the VRAM controller. The refresh cycle begins by locking the memory address output signals to point to the internal row portion of the address generator (SYSCLK edge 'A') for the duration of the cycle. This is done so that the memory address pins won't be bouncing around during refresh. At clock edge 'B', all of the  $\sim$ CAS pins are brought low. On the next clock edge, all  $\sim$ RAS pins are brought low. On clock edge 'G' the cycle ends and all  $\sim$ CAS and  $\sim$ RAS signals are returned high. These refresh cycles will continue until the refresh burst count is reached. At that point, the refresh request goes away and the arbiter may acknowledge other requests.

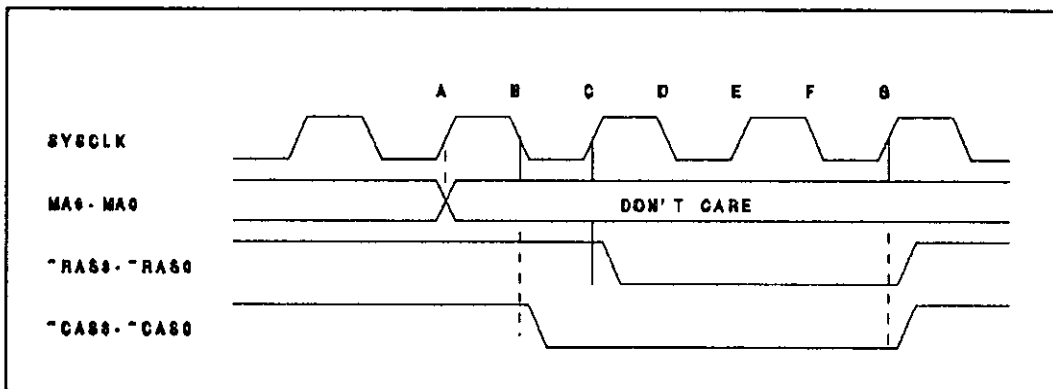


FIGURE 5-4 CAS-BEFORE-RAS REFRESH CYCLE



## 5.5 HOST DIRECT CYCLE

The ISC allows for several modes of memory access. The host direct mode of memory access, including block mode addressing, lets the host access the DRAM portion of memory randomly via the address and select input pins of the ISC. The row and column input address pins are multiplexed to the memory address output pins during a host direct access. The  $\sim$ CAS and  $\sim$ RAS control may come from either of several sources. The following table lists these sources and enabling control in order of decreasing priority:

MODE	$\sim$ RAS SOURCE	$\sim$ RAS SOURCE CONTROL BIT	$\sim$ CAS SOURCE	$\sim$ CAS SOURCE CONTROL BIT
OVERRIDE MODE	RAS OVERRIDE	CRA11	CAS OVERRIDE	CRA10
BLOCK MODE	BAR	CRB15	BAR	CRB15
EXTERNAL MODE	S1-S0	CRA13	S1-S0	CRA12

CRA: CONTROL REGISTER 'A'      CRB: CONTROL REGISTER 'B'      BAR: BLOCK ADDRESS REGISTER

TABLE 5-2 RAS AND CAS SOURCE CONTROL

A host direct cycle is initiated with a function select code of 3 (FS2-FS0=011) and the falling edge of  $\sim$ RAE. The  $\sim$ RDY tri-state output signal immediately goes from the high impedance state to a level high. The row address input and function select inputs are latched on the falling edge of  $\sim$ RAE and must meet setup and hold requirements. The column address inputs and select inputs are latched on the falling edge of  $\sim$ CAE and must also meet setup and hold requirements.

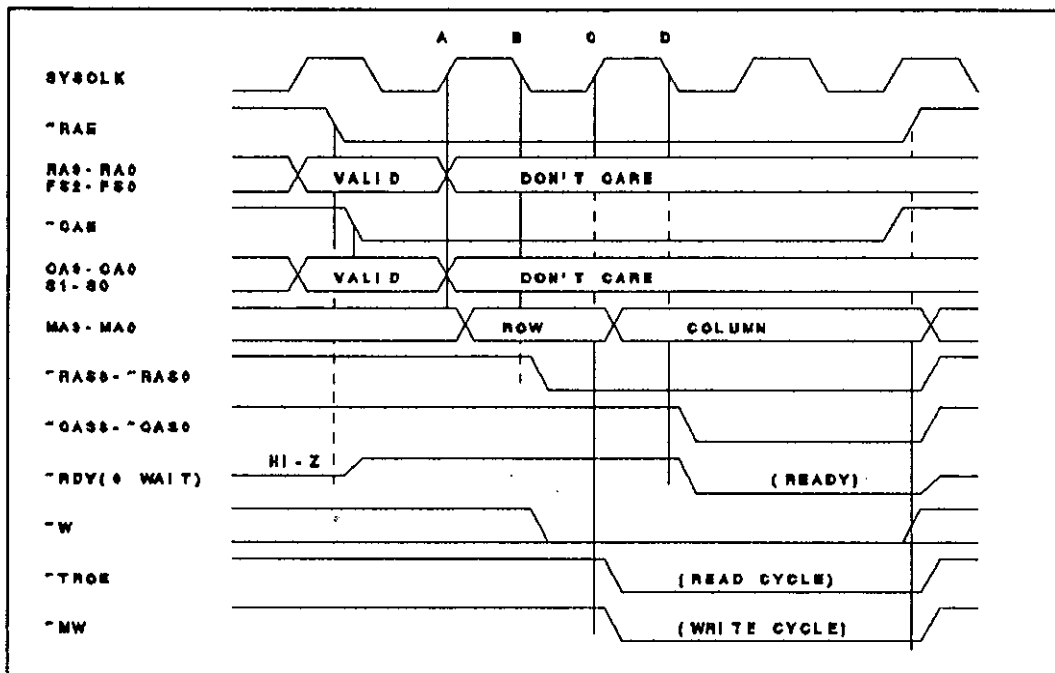


TABLE 5-5 HOST DIRECT OR X-Y INDIRECT CYCLE

Barring any conflicts with internally generated cycles, the ISC will begin the cycle on the next rising edge of SYSCLK (clock edge 'A'). At this time, the multiplexed memory address will point to the row address inputs

and the output signals  $\sim$ TROE and  $\sim$ MW will be forced to a high level. At SYSCLK edge 'B',  $\sim$ RAS is asserted low. The memory address output multiplexes to point to the column address inputs at clock edge 'C'. Also at clock edge 'C', the  $\sim$ TROE output signal is asserted low for a memory read or the  $\sim$ MW signal is asserted low for a memory write. At clock edge 'D', the  $\sim$ CAS output is asserted and  $\sim$ RDY transitions low when programmed for 0 wait states.

The cycle ends when the host drives the  $\sim$ RAE input high. When the cycle ends, all  $\sim$ RAS,  $\sim$ CAS,  $\sim$ TROE and  $\sim$ MW signals go high, the  $\sim$ RDY signal goes to a high impedance state and the multiplexed memory address becomes invalid.

## 5.6 X-Y INDIRECT CYCLE

In an X-Y indirect memory cycle, the ISC supplies the complete memory address from the X-Y address pointer. X-Y addressing allows the user to move through up to a 4 Meg memory address space with just a 4 bit function adjustment code. An X-Y address cycle is initiated with a function select code of 1 (FS2-FS0 = 001) and the falling edge of  $\sim$ RAE. The  $\sim$ W input pin determines the direction of the access. To begin addressing at a particular location, the desired start address can be programmed into the X-Y address registers.

An entire image may be addressed in-sequence with an X-Y function adjustment code of '+X'. In this mode, each X-Y cycle will access the next pixel until the end of a line. Once the end of the line has been reached, the next X-Y cycle will cause the address to wrap around to the next line. This wrap around ability is memory size sensitive, so be careful to program the ISC with the correct memory size that you are using. Also, the address will wrap around to zero and NOT to your starting address (unless your starting address is zero). X-Y addressing is also useful for line drawing, region of interest data moves and when matched with automatic display update addressing, providing the active line-time addressing for real-time processing. By varying the row and column step sizes, various physical memory architectures may be transformed from a row/column orientation to a pixel/row orientation. The programmable stepsize also allows the user to move about in memory in steps greater than one.

The timing of an X-Y indirect cycle is shown in figure 5-5 and is similar to that of a host direct cycle.

## 5.7 SHIFT-REGISTER READ OR WRITE TRANSFER CYCLE

A shift-register transfer cycle is an access that is initiated by the host processor. A function select code of 4 determines a write transfer and a function select code of 5 determines a read transfer. The cycle begins on the falling edge of  $\sim$ RAE. A shift register read transfer copies a row of DRAM data, specified by the address at pins RA9-RA0, to serial access memory, circularly shifted by the number columns specified by the address at pins CA9-CA0. A shift register write transfer copies the contents of serial access memory into the row of DRAM specified by the address at pins RA9-RA0 and circularly shifted by the number columns specified by the address at pins CA9-CA0. The source of the row and column address strobes is programmable and shown in table 5-2.

The timing for a shift-register transfer cycle is shown in figure 5-6. The host initiates the cycle by driving  $\sim$ RAE low. The row address input and the function select input are latched on the falling edge of  $\sim$ RAE and the  $\sim$ RDY output pin leaves its high impedance state and is asserted high. The column address input and the select input are latched on the falling edge of  $\sim$ CAE. This signal also allows the column address strobes to be asserted later in the cycle. At rising SYSCLK edge 'A', the memory address output points to the address

contained in the row address latch, the output signal  $\sim$ TROE is asserted low and if this is a write transfer, the  $\sim$ W output signal is asserted low. At clock edge 'B', the row address strobe(s) become active. At clock edge 'C', the multiplexed memory address points to the column address latch. The column address strobe(s) become active after clock edge 'D', as well as a 0 wait state ready. The output signal  $\sim$ TROE becomes inactive after clock edge 'F' and the entire cycle ends when the host drives  $\sim$ RAE high again.

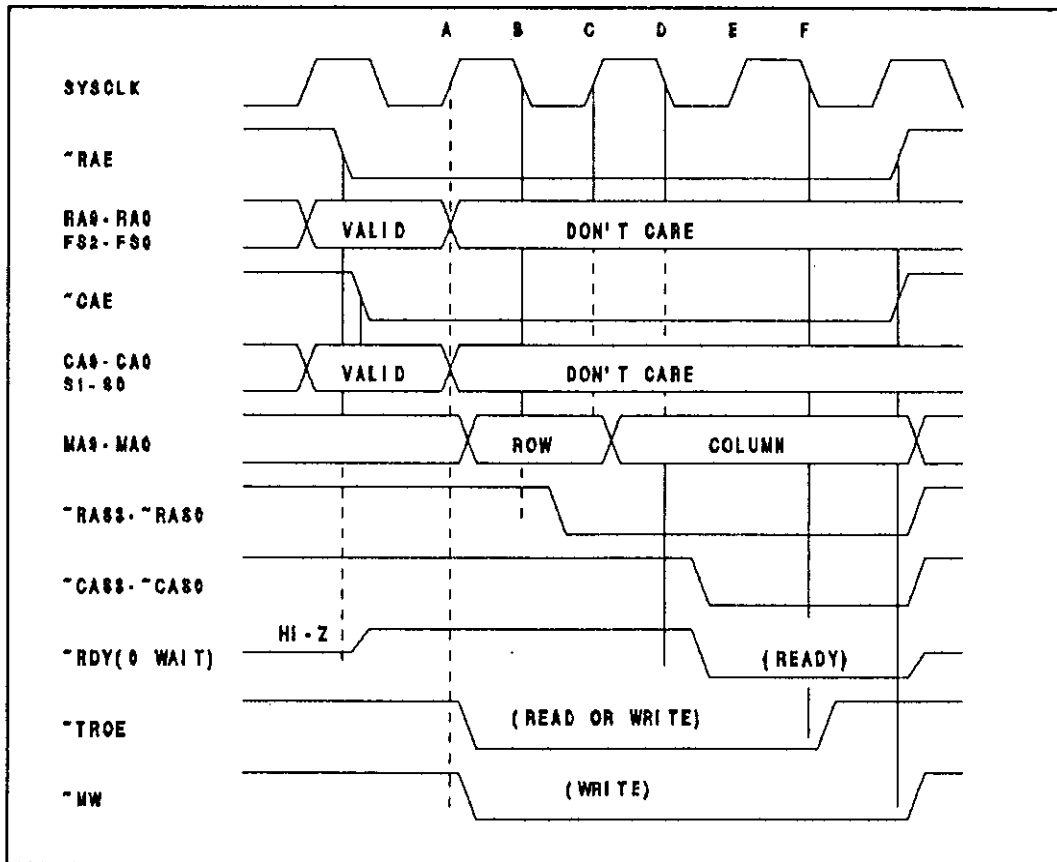


FIGURE 5-6 SHIFT-REGISTER READ OR WRITE TRANSFER CYCLE

## 5.7 FAST PAGE MODE

The ISC provides the ability to access memory in fast page mode. This feature is available in both host direct access mode and X-Y indirect addressing mode and is required for real-time access mode. This feature works by allowing a direct path from the  $\sim$ CAE input pin to the column address strobe output via a minimum logic delay path in the ISC. Essentially, the user supplies the column address strobe timing signals. The selection of column address strobe is still selectable in this mode according to the values in table 5-2. It is left to the user to ensure that a row boundary is not crossed during a fast page cycle. Used with a host direct access cycle, the user must ensure a timely and stable column address and select input. During an X-Y fast page mode cycle, the row function adjust code must not be altered and the column address must not be allowed to wrap around to the next row. If a final column adjust is to increment (or decrement) to another row, both  $\sim$ RAE and  $\sim$ CAE must go high within the same SYSCLK cycle.

Figure 5-7 shows a typical fast page mode cycle. The beginning of the cycle proceeds as normal until clock edge 'D' is reached. It is at this time that the ISC allows the input pin  $\sim$ CAE to directly control the

column address strobes. The input signal to pin  $\sim$ CAE must be synchronous with SYSCLK.

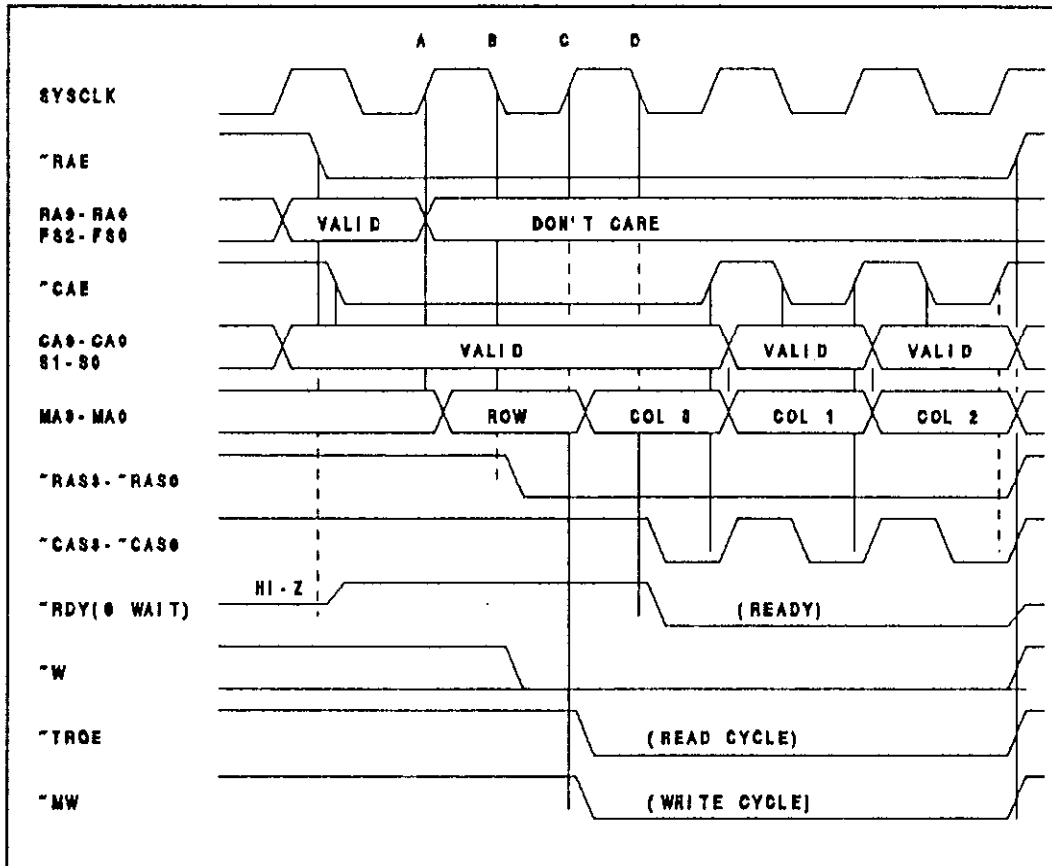


FIGURE 5-7 FAST PAGE MODE TIMING

## 5.9 READY INTERFACE

The ISC communicates the availability of memory and the ISC internal registers to the host via the active low ready signal at the  $\sim$ RDY pin. When the host processor asserts  $\sim$ RAE low, the  $\sim$ RDY pin immediately leaves its normal high impedance state and goes to a high level, signaling a NOT ready condition to the host. The active low ready signal is asserted at column address strobe time or after the appropriate number of wait states have been counted. If the ISC is busy with an internal cycle, the arbiter will hold off the host processor with the  $\sim$ RDY pin in the NOT ready state until the internal cycle is terminated.

Figure 5-8 shows the four possible ready conditions. The number of wait states inserted is varied by programming control register 'A', bits 6 and 7 (see figure 4-1 and table 4-4). Each wait state is half a SYSCLK cycle long. The start of wait states is relative to the falling edge of the column address strobe.

The host processor ends the cycle by asserting  $\sim$ RAE high. At this time, the  $\sim$ RDY output pin will go back to the high impedance state.

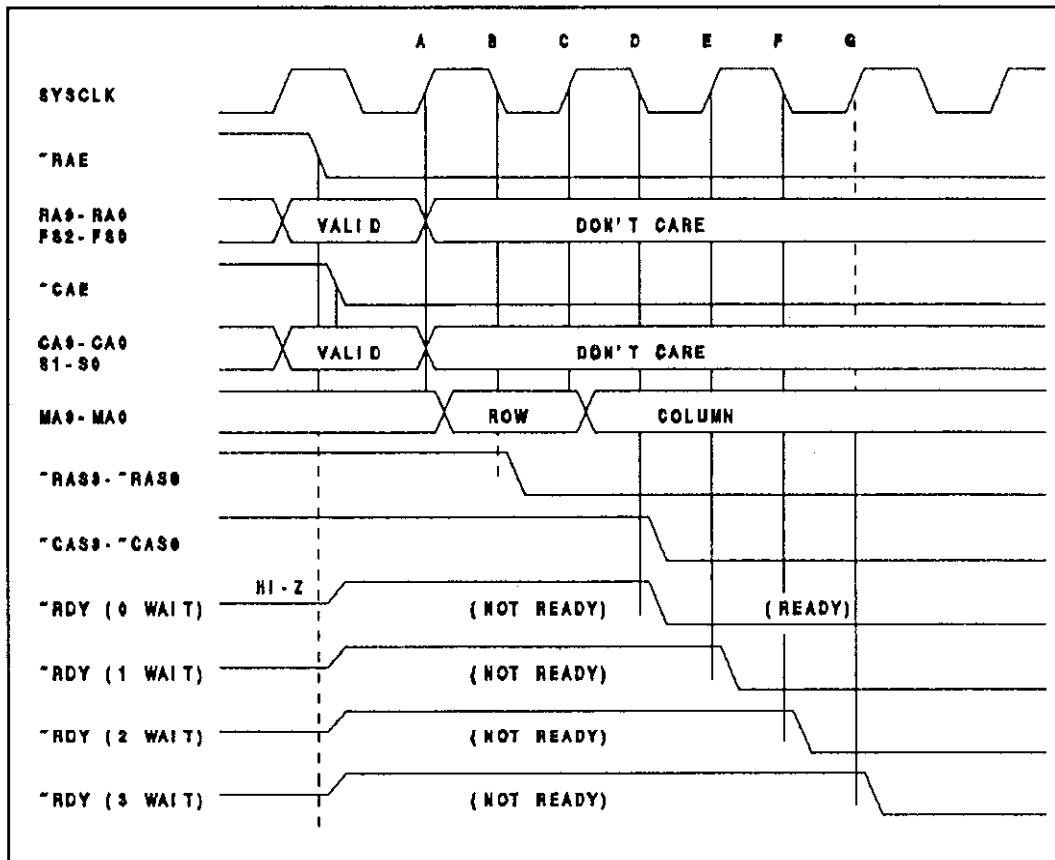


FIGURE 5-8 READY TIMING WITH WAIT STATES

## 5.10 RESET AND INITIAL SETUP

The ISC requires that the  $\sim$ RESET pin be held low for a minimum of 2 SYSCLK cycles. After the release of the  $\sim$ RESET pin, the system should wait a minimum of 512 VIDCLK cycles plus 52 SYSCLK cycles for the ISC to wake up the VRAM. Reset places the internal registers and the output pins of the ISC into a defined state. Table 4-2 lists the state of the host accessible registers after reset and table 5-3 lists the state of the output pins immediately after reset.

After reset, the ISC is programmed to perform eight CAS-before-RAS refreshes every 513 video clock cycles, that is, the burst refresh length is programmed for eight refreshes per burst and the horizontal total and horizontal start blank registers are programmed with a value of 512.

Until the host reprograms the ISC, a horizontal sync and a horizontal blank will occur every 513 VIDCLK cycles and will each last for 129 VIDCLK cycles. A vertical sync and a vertical blank will occur every 513 horizontal lines and will each last for 129 horizontal lines. Composite sync will follow the horizontal sync signal. After every eight horizontal line counts, a display update of memory row zero will occur.

PIN NAME	RESET STATE
~RDY	HIGH IMPEDANCE
~INT	LOGIC HIGH LEVEL
~ICREQ	LOGIC HIGH LEVEL
HD7-HD0	HIGH IMPEDANCE
MA9-MA0	LOGIC LOW LEVEL
~TROE	LOGIC HIGH LEVEL
~MW	LOGIC HIGH LEVEL
~RAS3-~RAS0	LOGIC HIGH LEVEL
~CAS3-~CAS0	LOGIC HIGH LEVEL
~HSYNC	LOGIC HIGH LEVEL
~CSYNC	LOGIC HIGH LEVEL
~VSYNC	LOGIC HIGH LEVEL
~VRST	LOGIC HIGH LEVEL
~CBLNK	LOGIC LOW LEVEL

TABLE 5-3 OUTPUT SIGNALS AFTER RESET

## 6 DISPLAY AND ACQUIRE CONTROL

The ISC can automatically acquire a frame of video data into video RAM via its auto-acquire mechanism. The ISC creates the following signals necessary for display control and frame synchronization:  $\sim$ HSYNC,  $\sim$ CSYNC,  $\sim$ VSYNC,  $\sim$ VRST and  $\sim$ CBLANK. These signals are fully synchronous to the user supplied video clock, VIDCLK. The duration and position of these signals, with the exception of composite sync, are fully programmable via the eight host accessible video timing registers. The pulse widths of the composite sync signal are automatically calculated by the ISC and are transparent to the user. The three video counters, horizontal counter, vertical counter and composite sync counter, are observable by the host. These counters are clocked by the video clock and their values compared to the sync and blank latches to determine the position and duration of these signals.

The ISC can also synchronize itself to another ISC or an external video source via the input signals  $\sim$ XHSYNC and  $\sim$ XVRST.

The ISC may also be programmed to create a flag to the status register and an interrupt to the host at a user programmable video line number. The register that stores this value is the Vertical Interrupt register.

The ISC supports the following video features:

- Auto-acquisition
- Interlaced operation (NTSC or PAL)
- Non-interlaced operation
- External horizontal sync only
- External vertical sync only
- External horizontal and vertical sync
- Programmable sync and blanking intervals
- Vertical blankless acquisition (useful for line scan)
- Automatic composite sync value calculations

### 6.1 AUTO-ACQUISITION

The acquisition trigger, pin 31, enables the automatic display and acquire update generation in a special manner. When this pin is held high, no acquisitions or displays are performed unless this signal had gone low in the previous frame. If this is the case, then the current frame will be displayed/acquired and no further frames will be displayed/acquired until pin 31 is brought low again. If pin 31 is held low, the ISC will display/acquire continuously until the pin is brought high. If this is the case, the current frame will be displayed/acquired and no further frames will be displayed/acquired until pin 31 goes low again. Pin 31 must be held low for continuous display to a monitor. If this pin is toggled low then high in an inactive frame (ie. one that is not being acquired/displayed, the next available full frame of data will be acquired. If pin 31 is toggled within an active frame, the current frame and the following frame will be acquired/displayed. This feature is useful for processing multiple frames of data in real-time processing mode.

### 6.2 INTERNALLY GENERATED VIDEO SIGNALS

The ISC generates the following video signals:  $\sim$ HSYNC,  $\sim$ CSYNC,  $\sim$ VSYNC,  $\sim$ VRST and  $\sim$ CBLANK. There are two modes of video signal generation, interlaced and non-interlaced. Control register 'B', bit 4 enables and disables interlaced mode. Interlaced mode is further divided into NTSC standard and PAL

standard. Control register 'B', bit 3 controls the video standard.

The horizontal sync and horizontal blank signals are generated by comparing the value in the horizontal counter with the values in the horizontal total, end-sync, start-blank and end-blank registers. The horizontal counter increments its count on every rising edge of the video clock and is reset back to zero when the value in the horizontal total register is reached (see Figure 6-1). At this time, the horizontal sync signal transitions low. The horizontal sync signal will transition high when the value in the horizontal end-sync register is reached.

Composite blank consists of a horizontal blank portion and a vertical blank portion. Horizontal blank begins when the horizontal counter reaches the value in the horizontal start blank register and ends when the value in the horizontal end blank register is reached. In the example of figure 6-1,  $HTOT=N$ ,  $HESYNC=2$ ,  $HSBLNK=N-1$  and  $HEBLNK=3$ .

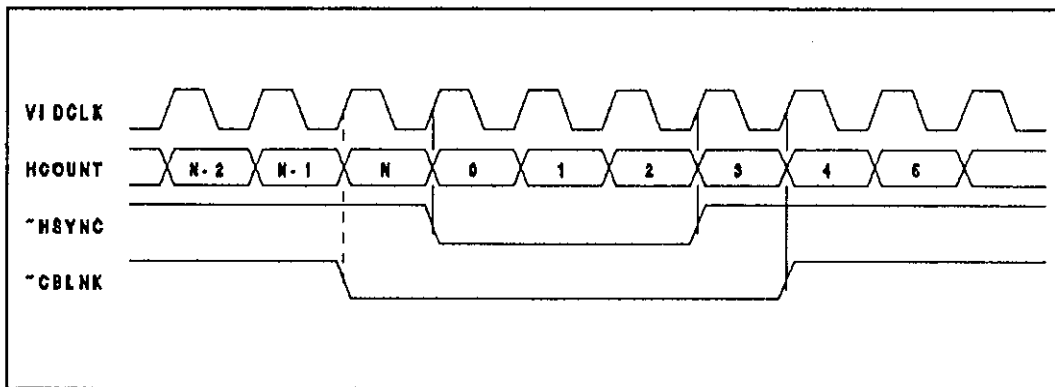


FIGURE 6-1 HORIZONTAL TIMING

### 6.2.1 NON-INTERLACED TIMING

In non-interlaced mode, the vertical signal generation is very much like that of the horizontal signal generation of above. The vertical sync and vertical blank signals are generated by comparing the value in the vertical counter with the values in the vertical total, end-sync, start-blank and end-blank registers. The vertical counter increments its count when the horizontal counter is reset and is reset back to zero when the value in the vertical total register is reached (see Figure 6-2). At this time, the vertical reset signal and the vertical sync signal transitions low. The vertical reset remains low for one horizontal line time. The vertical sync signal will transition high when the value in the vertical end-sync register is reached.

Vertical blank portion of composite blank begins when the vertical counter reaches the value in the vertical start blank register and ends when the value in the vertical end blank register is reached. In the example of figure 6-2,  $VTOT=M$ ,  $VESYNC=2$ ,  $VSBLNK=M-1$  and  $VEBLNK=3$ .

In non-interlaced mode, the composite sync signal becomes another horizontal sync output.



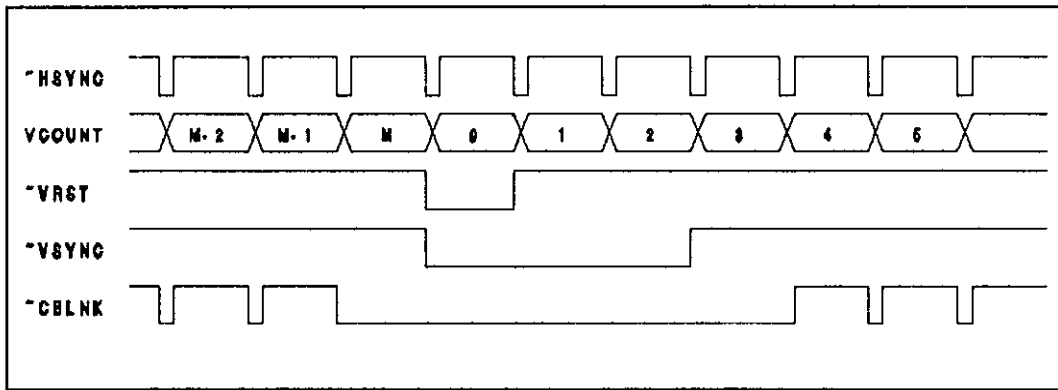


FIGURE 6-2 NON-INTERLACED VERTICAL TIMING

### 6.2.2 INTERLACED TIMING

In interlaced mode, the ISC behaves as a field machine. Vertical reset is generated once at the beginning of each frame when the vertical counter is reset to zero. The vertical counter resets when the value in the vertical total register is reached AND either horizontal sync or the horizontal mid-line occurs. The counter alternates resetting on horizontal sync and horizontal mid-line strobe each field. In the case of NTSC timing, the vertical counter is reset at horizontal sync time before the beginning of the first field and reset at horizontal mid-line time before the beginning of the second field. Also, the vertical reset signal is asserted low when the vertical counter reset is concurrent with horizontal sync and asserted high one-half line time latter. In the case of PAL timing, the vertical counter is reset at horizontal mid-line time before the beginning of the first field and reset at horizontal sync time before the beginning of the second field. Also, the vertical reset signal is asserted low when the vertical counter reset is concurrent with horizontal mid-line and asserted high one-half line time latter.

In interlaced mode, the value to be programmed into the vertical total register is:

$$VTOTAL = (\text{total number of lines in a FRAME} - 1) / 2$$

The vertical counter counts from zero to VTOTAL but remains at the VTOTAL value for half of a line time. Thus, each field time is equivalent to  $VTOTAL + 1/2$  horizontal lines and a frame becomes  $2*(VTOTAL + 1/2)$  or  $2*VTOTAL + 1$  lines.

The vertical sync signal is asserted low three lines after the vertical counter is reset during NTSC mode and two and one-half lines after the vertical counter is reset during PAL mode. In both modes, the vertical sync signal returns high when the vertical counter reaches the value stored in the vertical end-sync register.

The vertical blank portion of composite blank behaves similarly to that in non-interlaced mode with the major exception that a half line blank is added to the beginning of an even field and at the end of an odd field. This insures that the odd field be displayed above the even field.

Figure 6-3 reveals the timing for NTSC video. The composite sync signal normally follows the horizontal sync signal until vertical reset. At this time, the composite sync signal consists of three lines of equalizing pulses, followed by three lines of broad or vertical pulses, followed by three more lines of equalizing pulses and then returning to horizontal sync pulses.

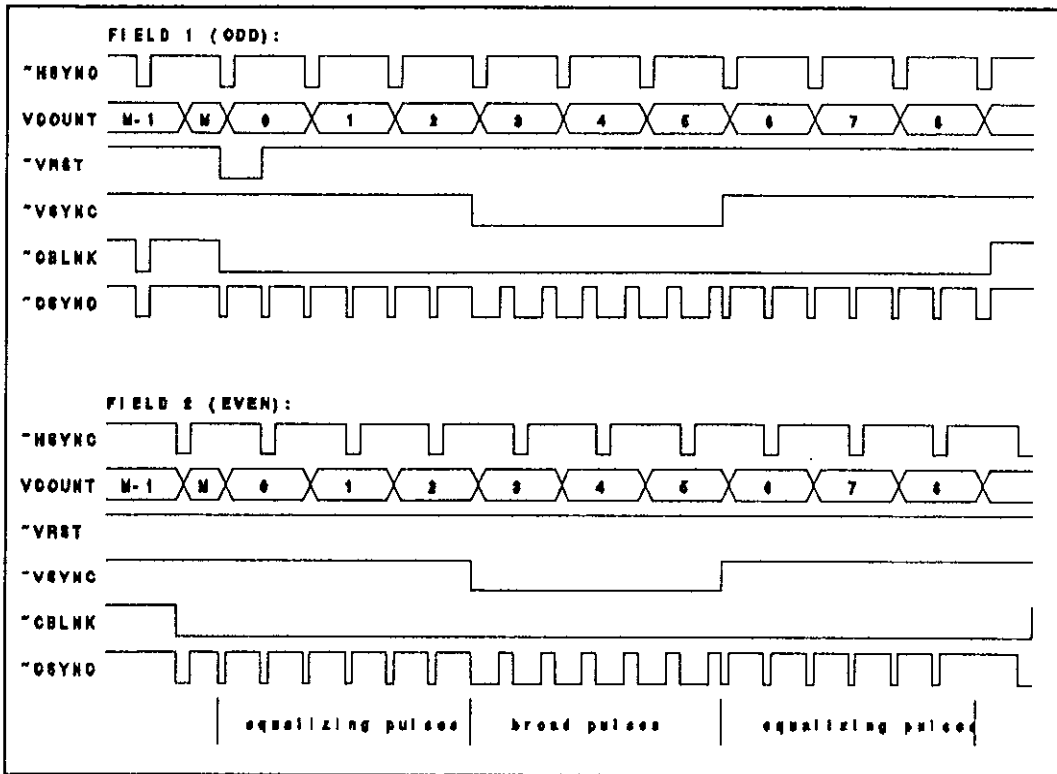


FIGURE 6-3 INTERLACED NTSC VIDEO TIMING

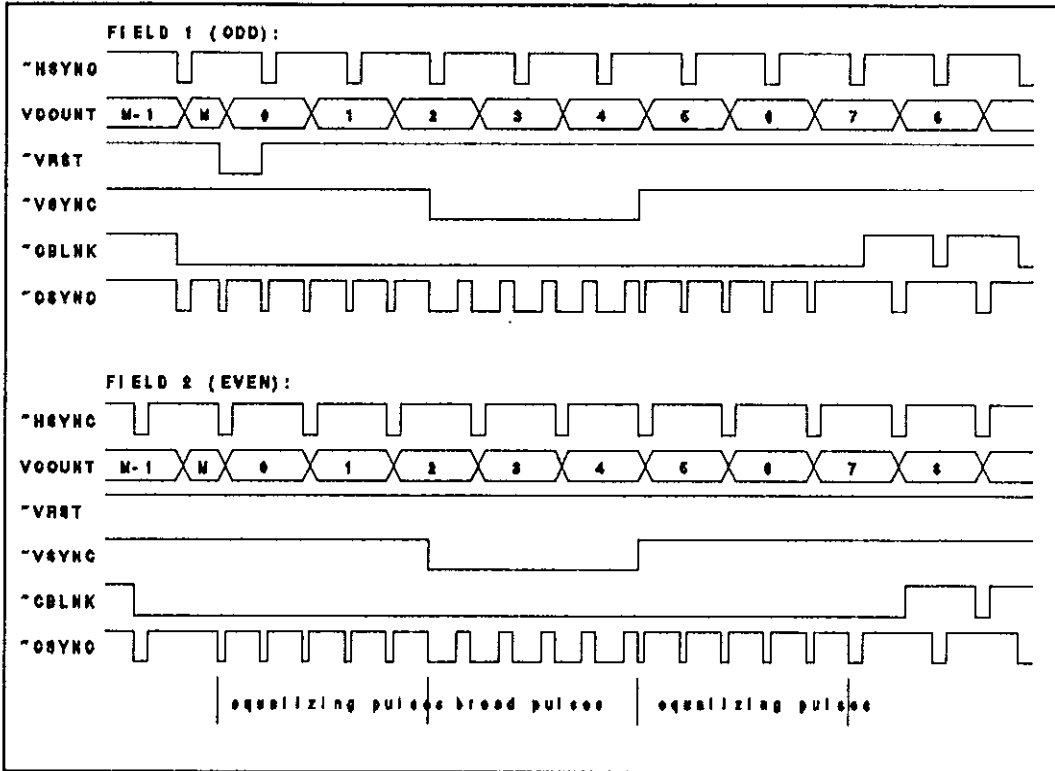


FIGURE 6-4 INTERLACED PAL TIMING

Figure 6-4 reveals the timing for PAL video. The composite sync signal normally follows the horizontal sync signal until vertical reset. At this time, the composite sync signal consists of two and one-half lines of equalizing pulses, followed by two and one-half lines of broad or vertical pulses, followed by two and one-half more lines of equalizing pulses and then returning to horizontal sync pulses.

The user need not worry about calculating the values for the composite sync equalizing and broad pulse width values. The ISC automatically calculates these values according to the following equations:

$$\text{EQ PULSE WIDTH} = \text{HSYNC PULSE WIDTH} / 2$$

$$\text{BROAD PULSE WIDTH} = (\text{HORIZ LINE LENGTH} / 2) - \text{HSYNC PULSE WIDTH}$$

### 6.3 EXTERNAL SYNC MODE

The ISC has independent sync signal inputs. This allows the ISC to synchronize to an external video source while still providing horizontal sync to a phase lock loop to generate VIDCLK. External horizontal synchronization is enabled by setting control register 'B', bit 2. External vertical synchronization is enabled by setting control register 'B', bit 1. The external sync inputs are event driven and are thus insensitive to pulse width, providing that the pulse duration is at least two VIDCLK cycles long. For best performance, the video clock should be harmonically related to horizontal sync.

Figure 6-5 shows the relationship of an external horizontal sync signal to the resulting horizontal counter reset and re-generated horizontal sync output. As can be seen in this figure, there is a two VIDCLK delay from the external horizontal sync going low, to the horizontal counter reset.

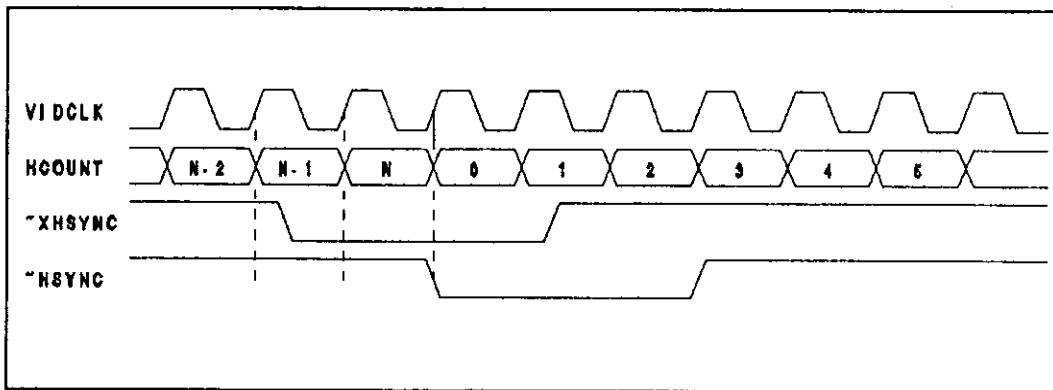


FIGURE 6-5 EXTERNAL HORIZONTAL SYNC TIMING

External vertical reset behaves differently depending on the video mode. In case 'A' of figure 6-6, the ISC is programmed for NTSC interlaced mode. In this case, the ISC will recognize an external vertical reset and clear the vertical counter within the window of horizontal sync to mid-line. If vertical reset occurs between mid-line and horizontal sync, the ISC will delay the resetting of the vertical counter until horizontal sync occurs. This is done to insure proper field alignment.

In case 'B' of figure 6-6, the ISC is programmed for PAL interlaced mode. In this case, the ISC will recognize an external vertical reset and clear the vertical counter within the window of mid-line to horizontal sync. If vertical reset occurs between horizontal sync and mid-line, the ISC will delay the resetting of the vertical counter until mid-line occurs.

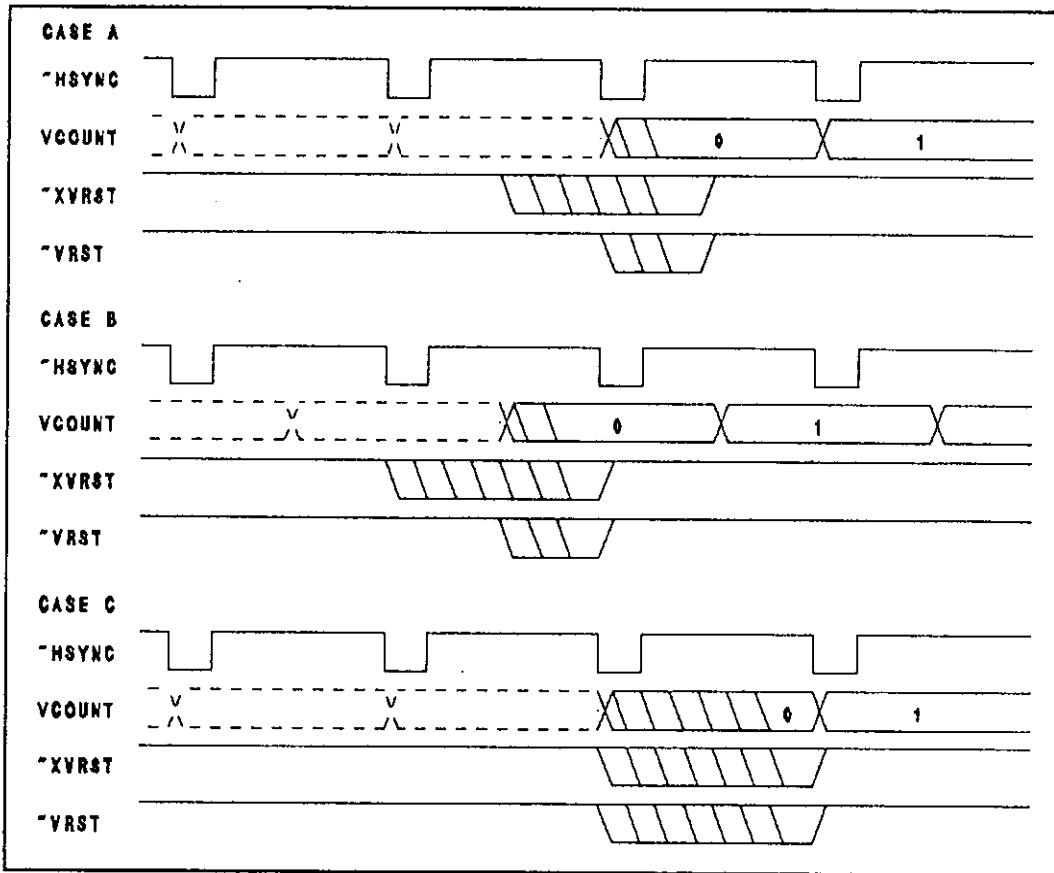


FIGURE 6-6 EXTERNAL VERTICAL TIMING

In case 'C' of figure 6-6, the ISC is programmed for non-interlaced mode. In this case, an external vertical reset may reset the vertical counter at any time.

Figure 6-7 shows the useful timing relationship between two ISC's in a master-slave configuration. The master horizontal sync and vertical reset signals are provided by ISC #1 to the external horizontal and vertical timing inputs of ISC #2. Two ISC's in this configuration form a tight relationship. The horizontal and vertical counters of ISC #2 will differ from that of ISC #1 by 2 VIDCLK cycles.

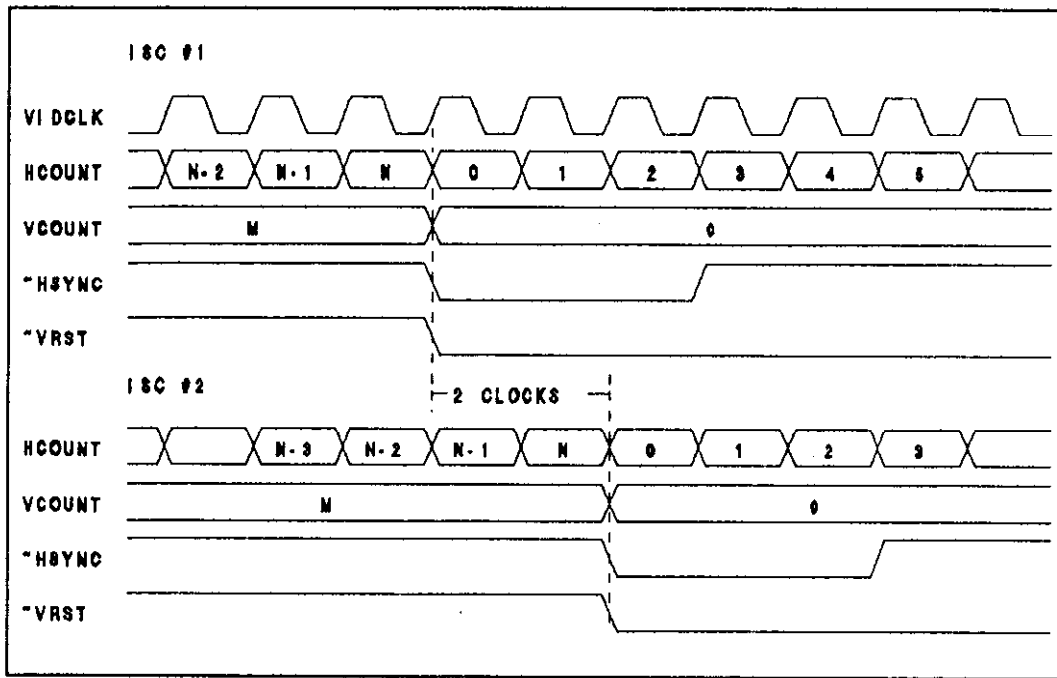


FIGURE 6-7 EXTERNAL SYNC TIMING WITH A TWO-ISC CONFIGURATION

## **7 SPECIFICATIONS**

**TBD**

## 8. REAL-TIME PROCESSING

There are many vision applications that require frame-rate processing. The ISC provides the control necessary to coordinate the serial access port and dynamic RAM port for in-place computations. The ISC provides the display or acquire updates at blank time and the fast page mode address generation during active line time.

The ISC is placed in real-time mode with a function select code of 6 (FS2-FS0=110). The host must not be allowed to access the ISC while the ISC is enabled for real-time processing. In order to fully synchronize memory access with pixel accesses, the pixel clock should be fed into the VIDCLK, SYSCLK and  $\sim$ CAE input pins of the ISC. The ISC should be programmed for 0 wait states in this mode. There must be a minimum of a two register delay in the processing data path to compensate for the initial two clock cycle delay of a DRAM access.

Figure 8-1 shows a typical data flow for a real-time display processor. The ALU must have a minimum of a two register pipeline delay. The serial port of VRAM and the ADC should be clocked on the same clock edge. In operation, the ISC will first transfer a row of data from the DRAM to the serial access memory (SAM) via a display update during blank time. When blank time ends and  $\sim$ RAE is asserted low, the ISC begins the fast page mode DRAM cycle. The same row address used in the display update is issued at  $\sim$ RAS time. The ISC then begins sending an incrementing the column address along with  $\sim$ CAS. When  $\sim$ CBLNK goes low again,  $\sim$ RAS should be held low for as many clock cycles as there are delays in the pipeline and then released. At this time the DRAM cycle ends and another display update is issued.

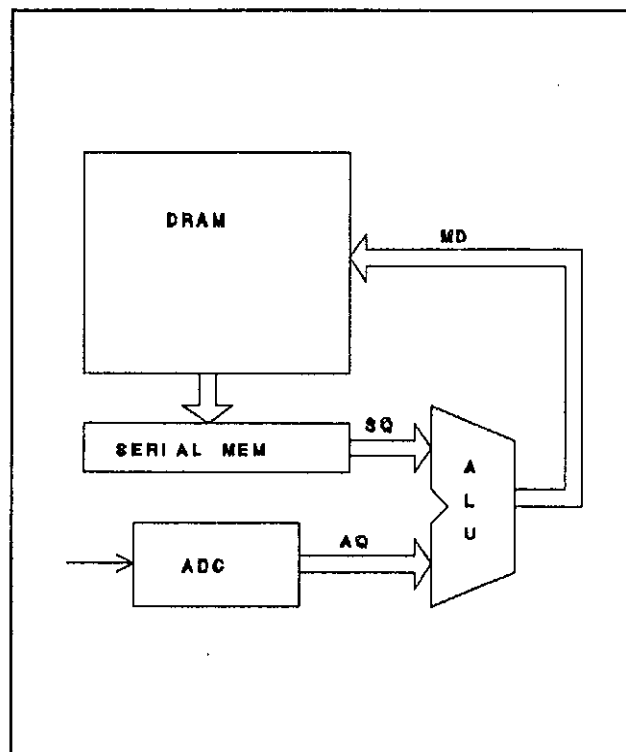


FIGURE 8-1 R-T DATA FLOW EXAMPLE

Figure 8-2 shows the timing signals for a four data sample example. The display update occurs during blank time and the column addressing begins two clock cycles after  $\sim$ RAE is asserted low. SQ is data from the serial access port. AQ is data from the analog to digital converter. MD is the data output from the ALU and input to the DRAM. SC is the serial port clock and  $\sim$ SE is the serial port enable.

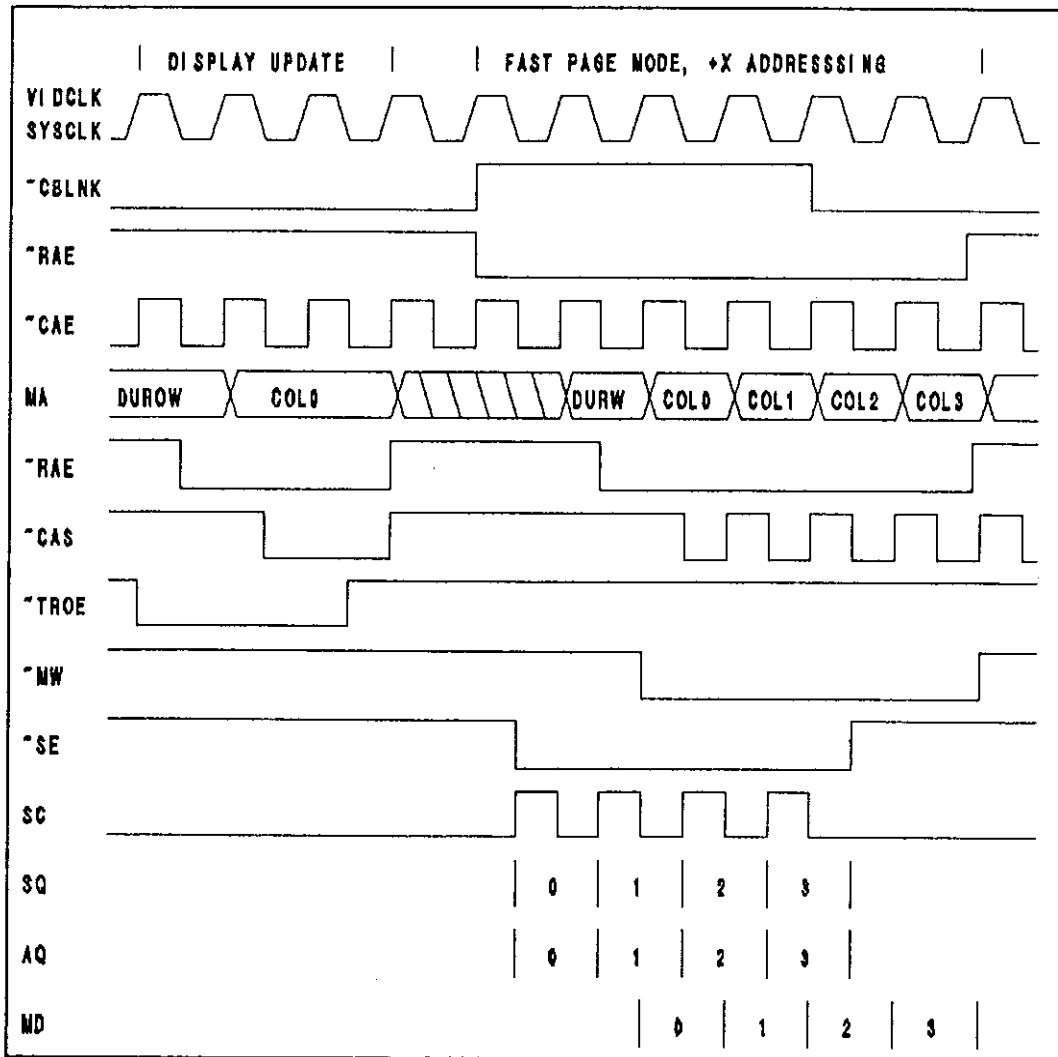


FIGURE 8-2 R-T TIMING EXAMPLE